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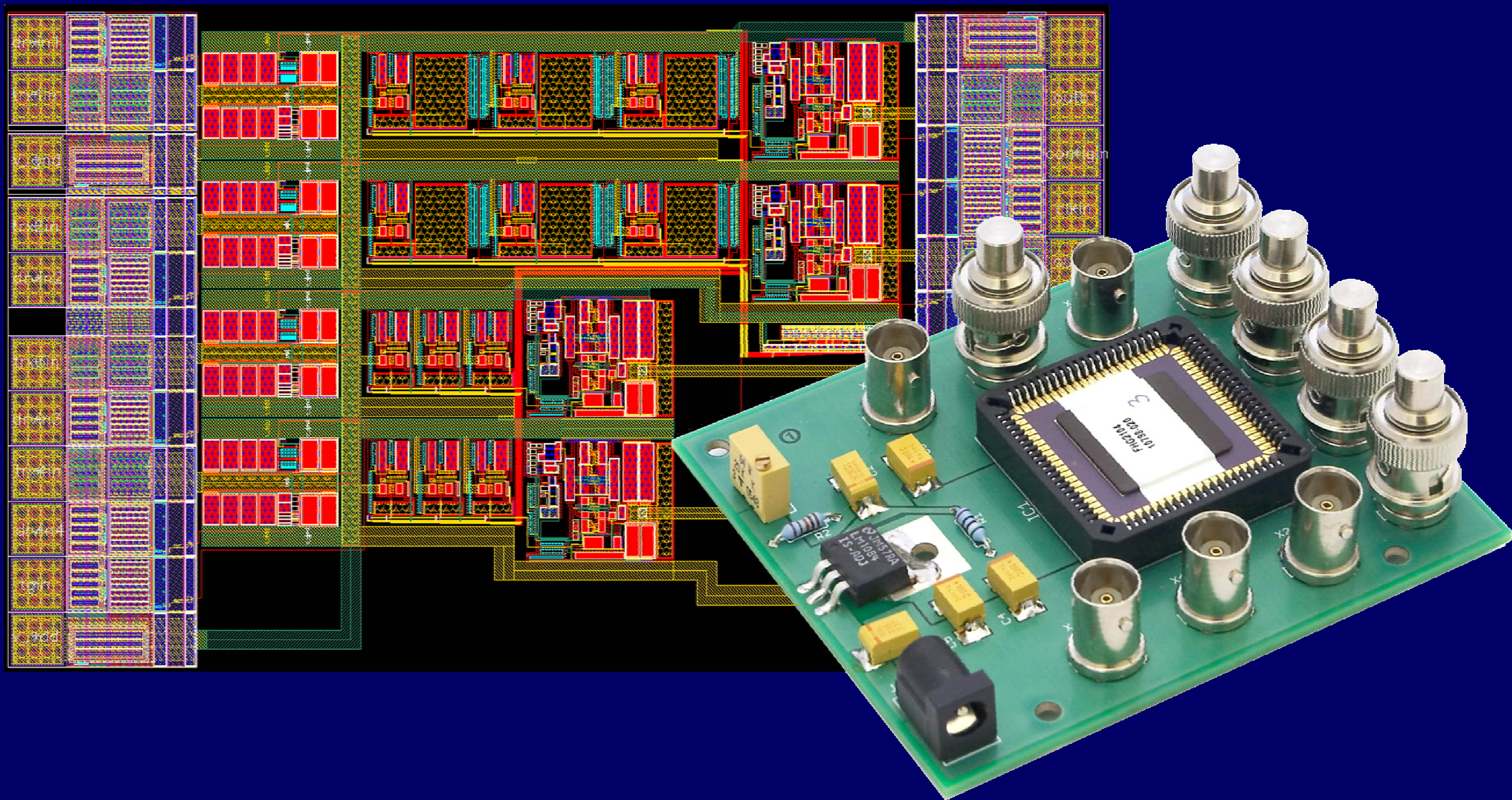
ASIC for an Integrated Ultrasonic Front End



The Applied Ultrasonics Laboratory

Motivation for ASIC design

- Multi-channel ultrasonic systems need ASIC implementation

Reason: when number of channels increase, the system based on discrete components features unacceptable big size, weight and cost

Motivation for ASIC design

- Develop and test electronic components for an integrated ultrasonic front end ASIC

ASIC1 was implemented to fulfil this task

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Motivation for ASIC design

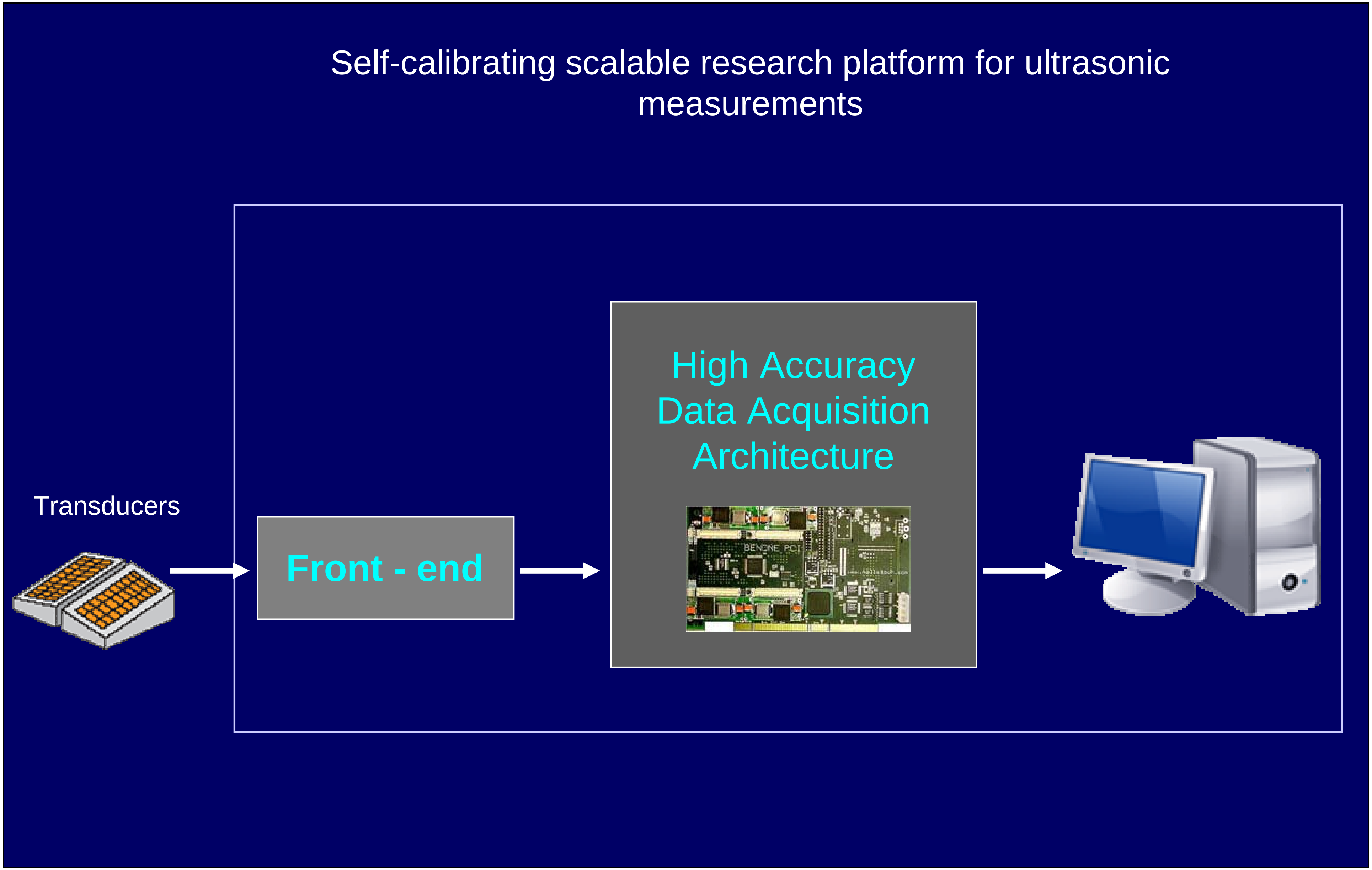
- Implement an integrated analogue front end for Self-calibrating scalable research platform for ultrasonic measurements [1] based on High Accuracy Data Acquisition Architecture for Ultrasonic Imaging [2]

ASIC2 was implemented to fulfil this task

[1] A. N. Kalashnikov, V.G. Ivchenko, R. E. Challis, W. Chen, “Self-calibrating scalable research platform for ultrasonic measurements in chemical and biological reactors”, in Proc. IEEE Instrum. Measurem. Conf., 2007

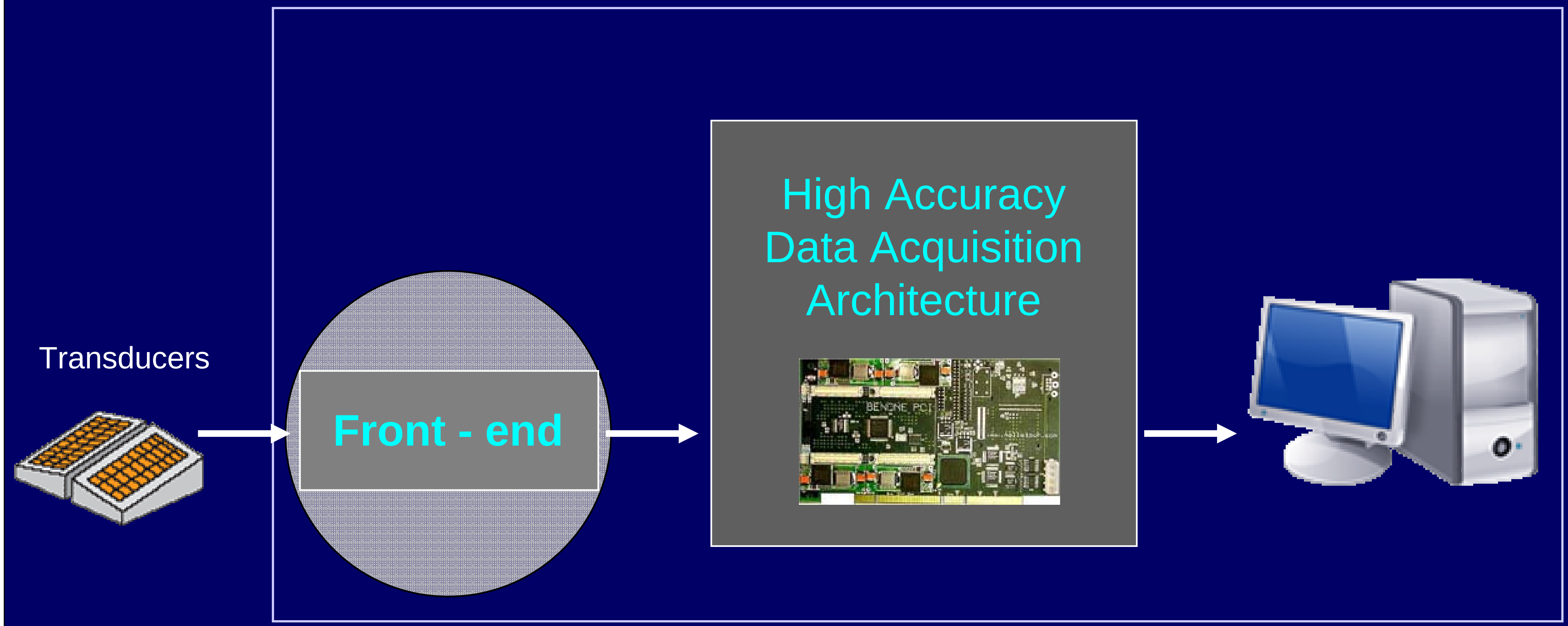
[2] A. N. Kalashnikov, V. Ivchenko, R. E. Challis and B. R. Hayes-Gill, “High Accuracy Data Acquisition Architectures for Ultrasonic Imaging”, accepted for Special Issue on High Resolution Ultrasonic Imaging in Industrial, Material and Biomaterial Applications of IEEE Trans. Ultrasonics, Ferroel., Freq.Control on 20 July 2006 (TUFFC-01587-2006)

ASIC application and Background



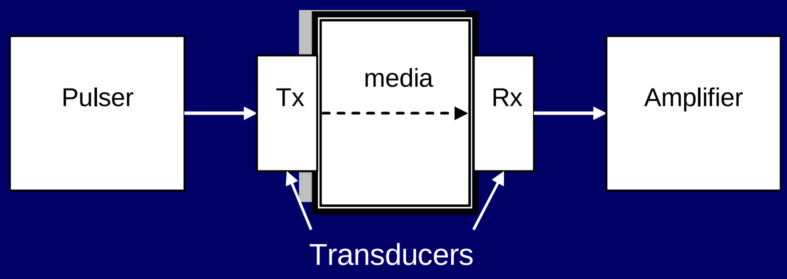
ASIC application and Background

Self-calibrating scalable research platform for ultrasonic measurements

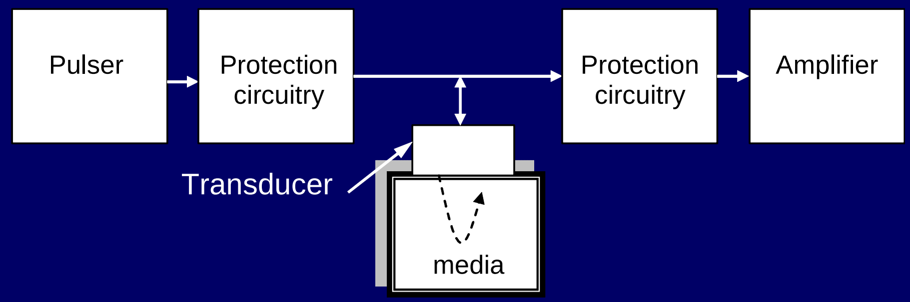


ASIC application and Background

Supported operating modes of front-end



Through pulse mode



Pulse-echo mode

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ASIC application and Background

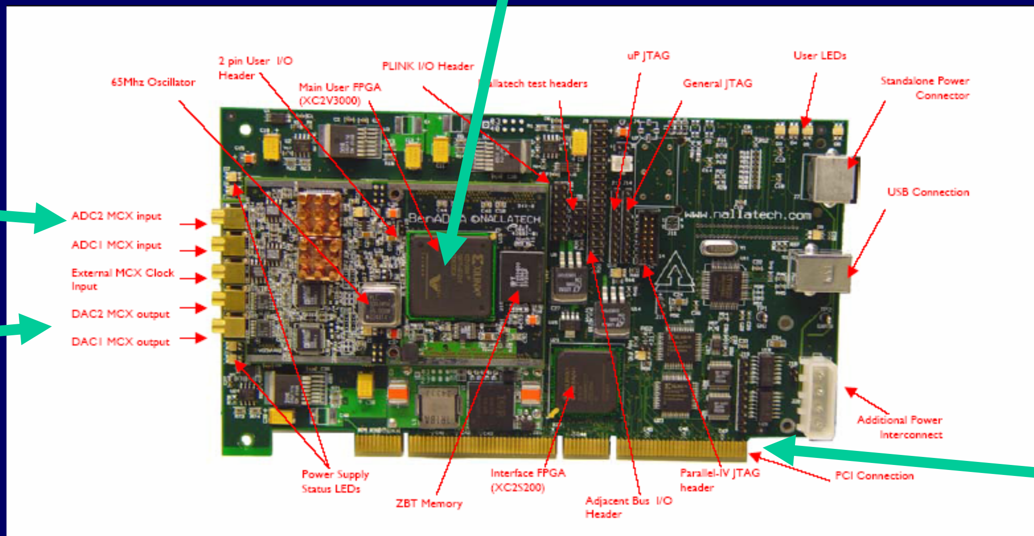
Implementation of Self-calibrating scalable research platform for ultrasonic measurements

<u>Hardware platform</u>

FPGA

2 x ADCs

2 x DACs

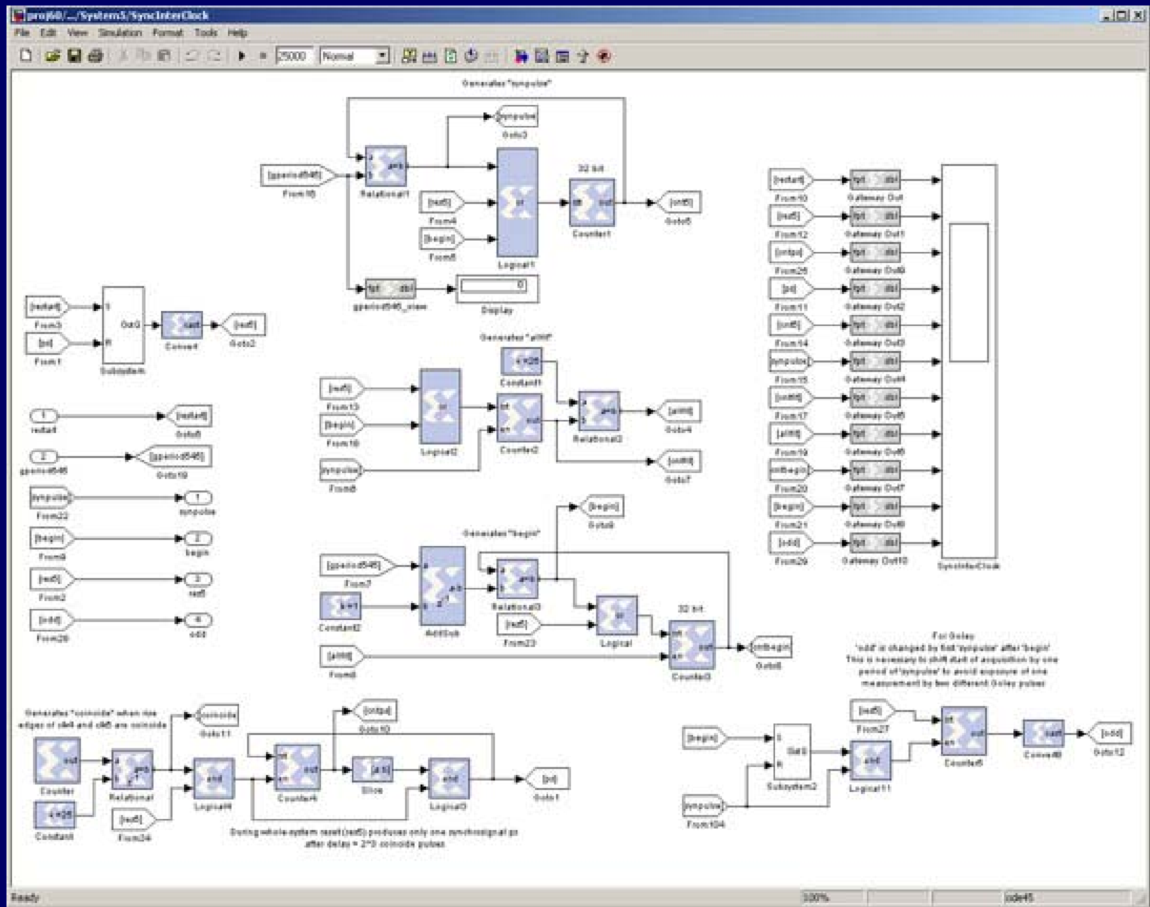


PCI Interface

Xilinx FPGA Development Kit

ASIC application and Background

Implementation of Self-calibrating scalable research platform for ultrasonic measurements

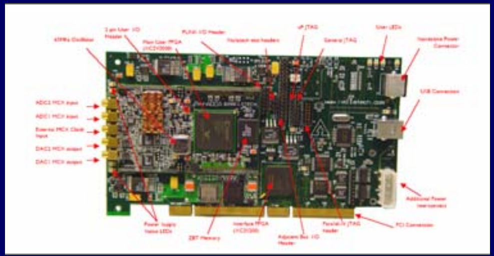


Design environment – Xilinx System Generator

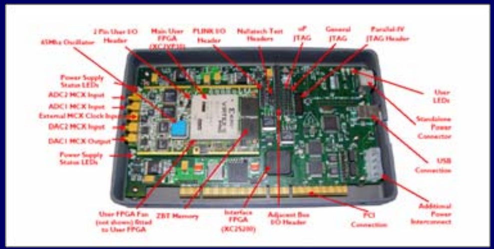
ASIC application and Background

Scalability and portability of the platform

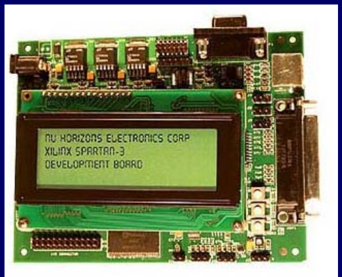
<u>Three boards were used to port the design:</u>



- Nallatech Virtex II XtremeDSP Development Kit-II



- Nallatech Virtex II Pro XtremeDSP Development Kit Pro



- Nu Horizons Electronics Spartan3 400 Evaluation Platform HW-AFX-SP3-400

ASIC application and Background

Problems of typical ultrasonic instrument

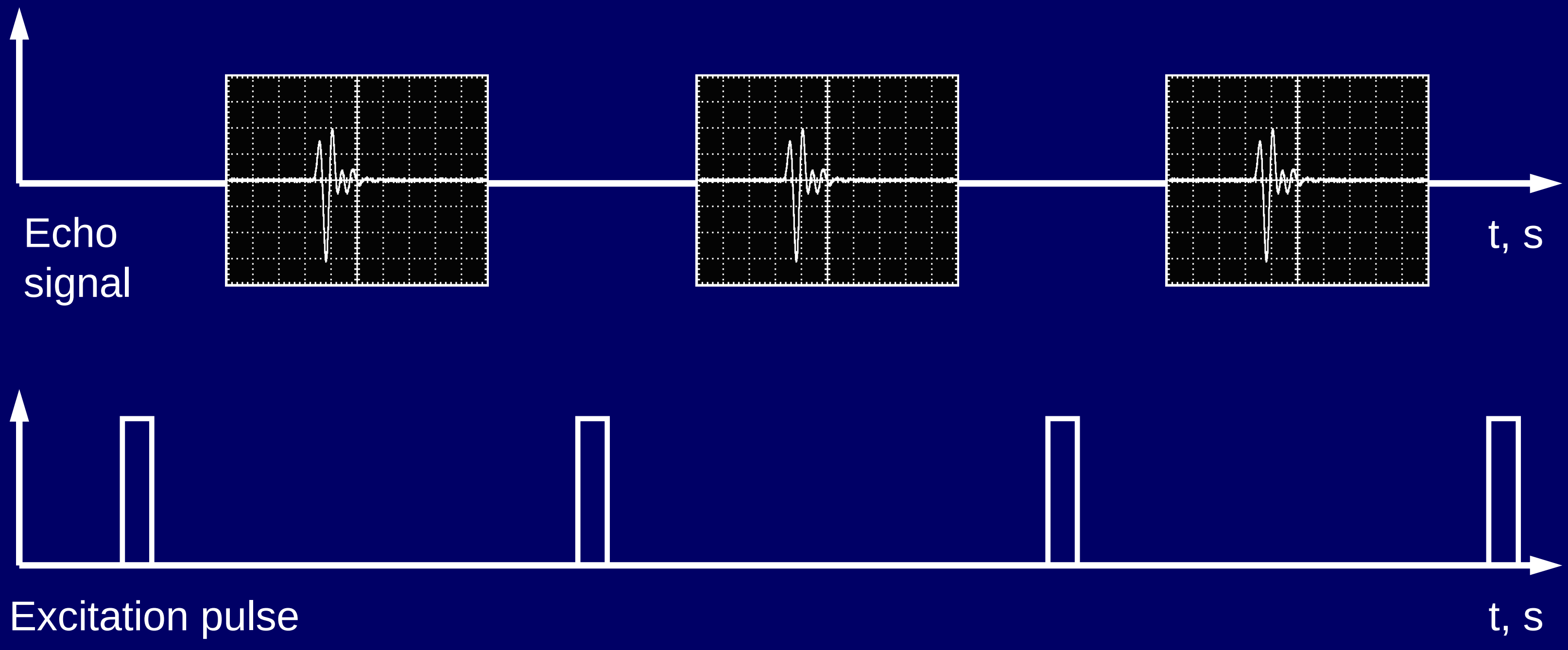
resolved in the new architecture

- Frame jitter
- Long averaging time
- Low time domain resolution
- Environmental influence on time domain precision

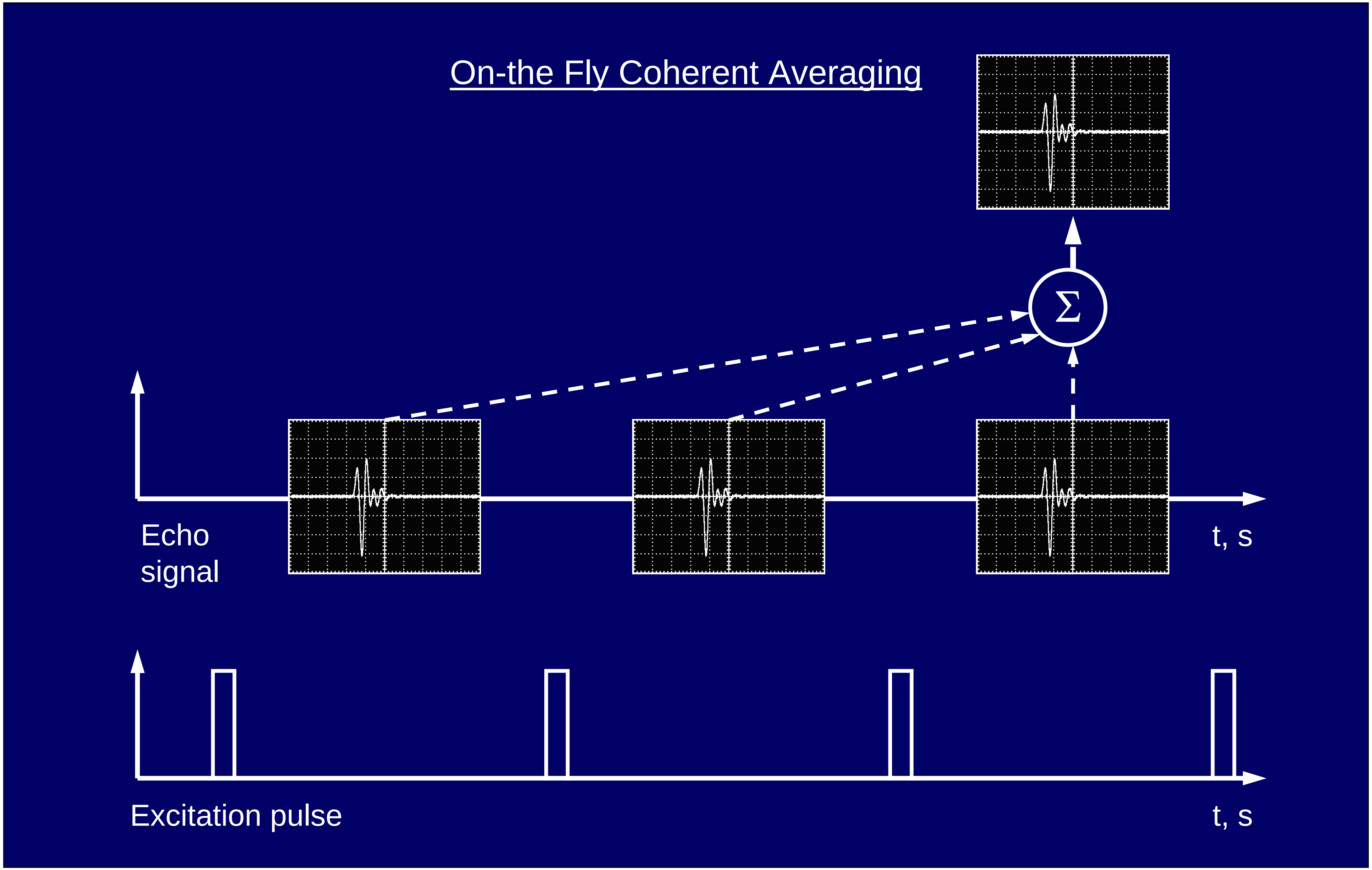
ASIC application and Background

Main features implemented in new architecture:

On-the Fly Coherent Averaging



ASIC application and Background



ASIC application and Background

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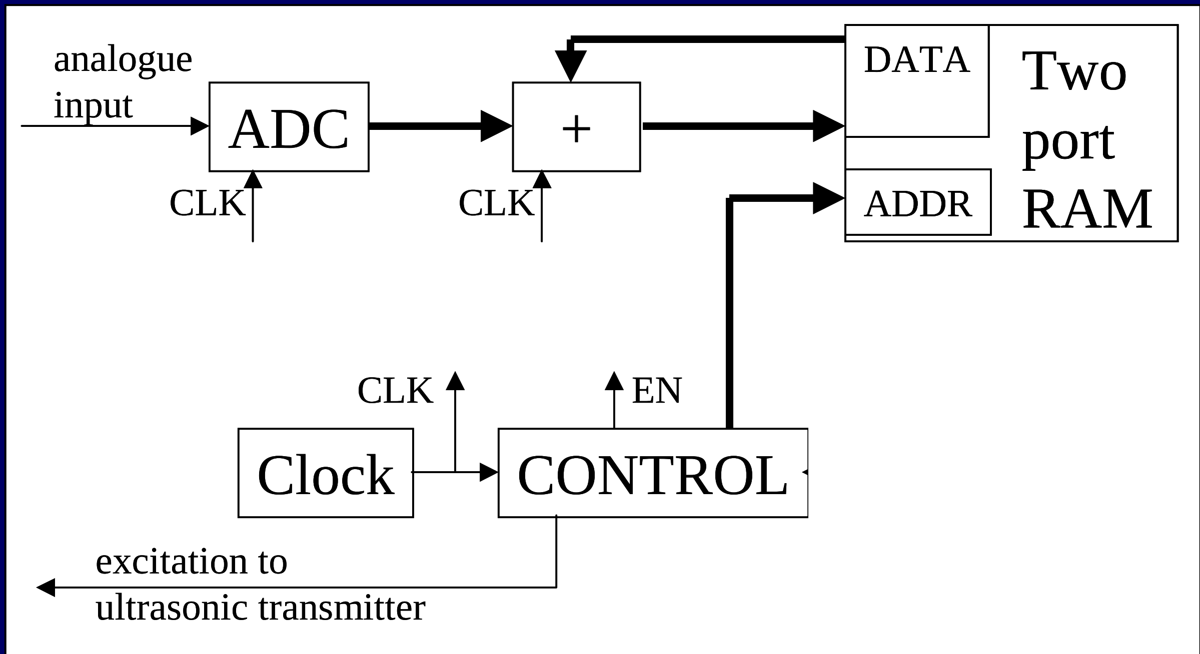
On-the Fly Coherent Averaging



On-the-fly averaging architecture

ASIC application and Background

Main features implemented in new architecture:

No Frame Jitter

- Jitter noise arises from random timing errors during the signal sampling process.
- Jitter can occur:

i) in the timing of the start of the frame or

ii) in the intervals between individual samples within a given frame.

- In practice frame jitter is the dominant source of error, whereas individual sample jitter can be neglected [3,4]

[3] A. N. Kalashnikov, R. E. Challis, Unwin M. E. and A. K. Holmes, “Effects of frame jitter in data acquisition systems”, IEEE Trans. Instrum. Measur., vol.54, pp.2177-2183, 2005.

[4] A.N. Kalashnikov and R. E. Challis, “Errors and uncertainties in the measurement of ultrasonic wave attenuation and phase velocity”, IEEE Trans. Ultrason., Ferroel., Freq.Control, vol.52, pp.1754-1768, 2005.

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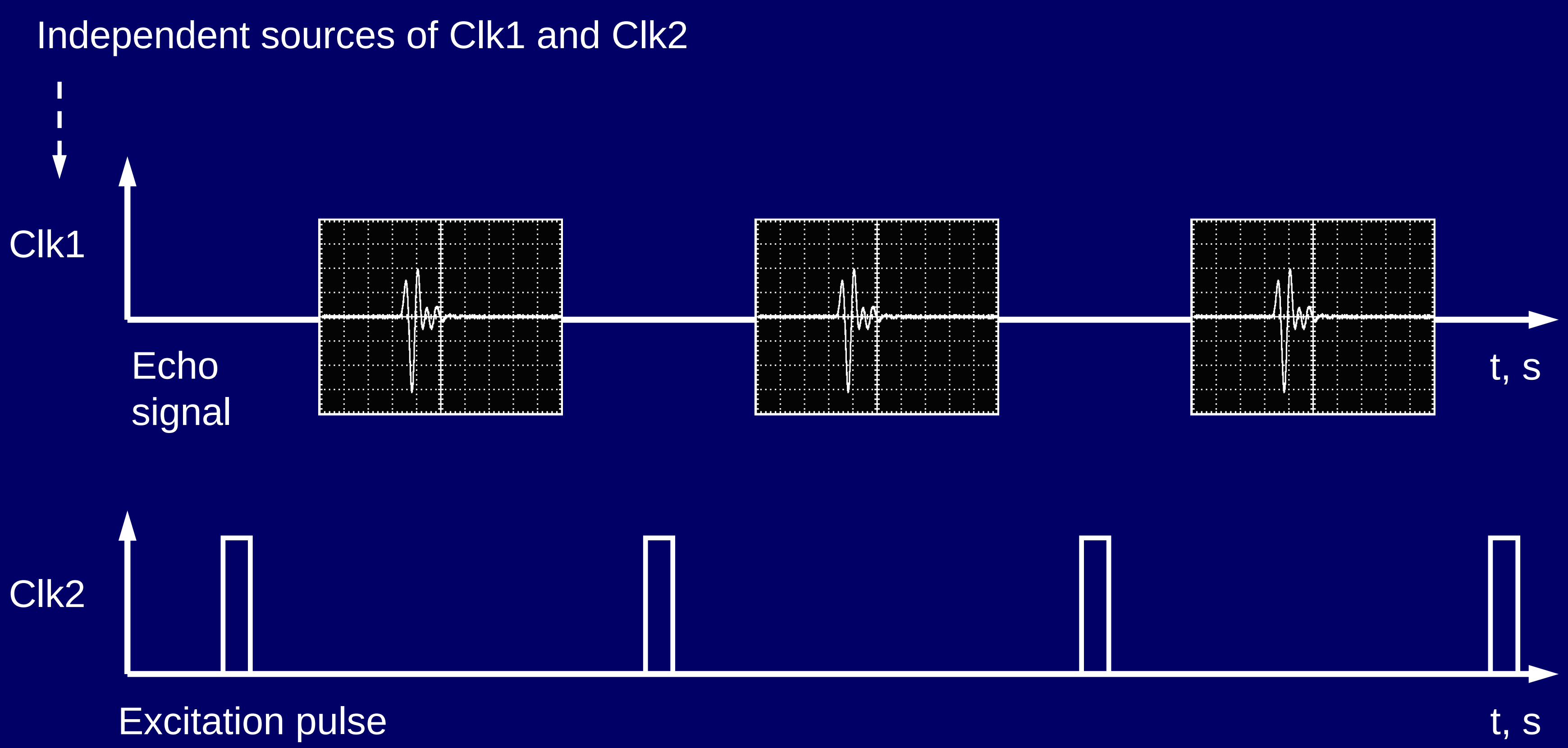
ASIC application and Background

Main features implemented in new architecture:

<u>No Frame Jitter</u>

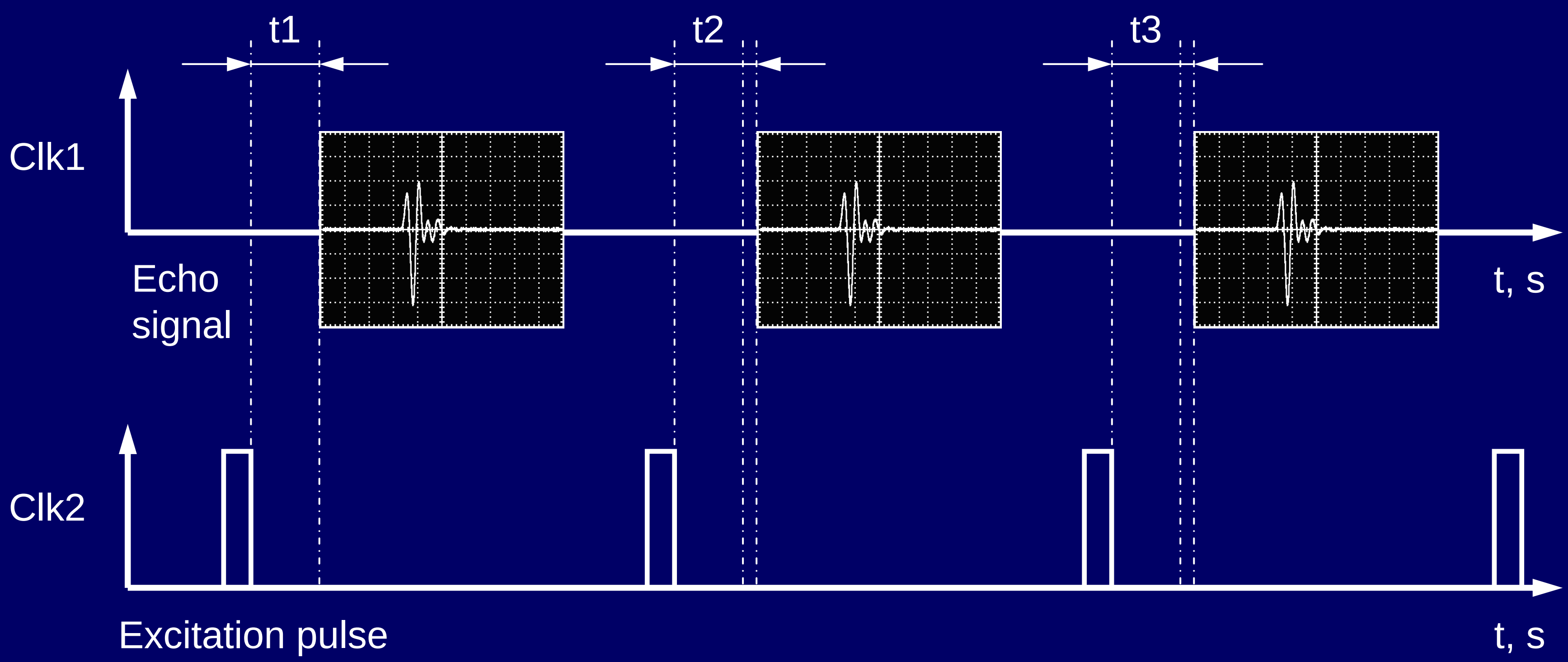


ASIC application and Background

Main features implemented in new architecture:

No Frame Jitter

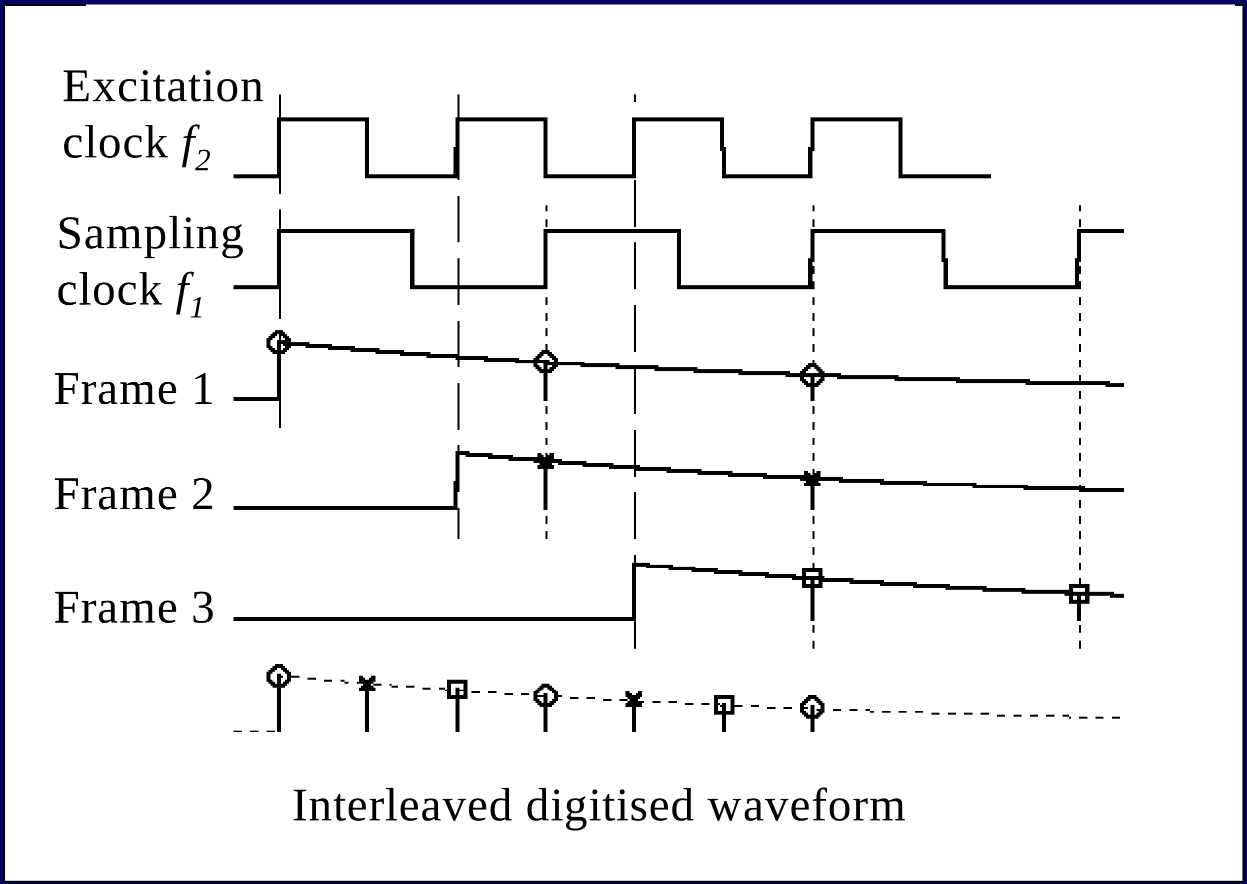
If t1≠ t2 ≠ t3 frame jitter is present



ASIC application and Background

Main features implemented in new architecture:

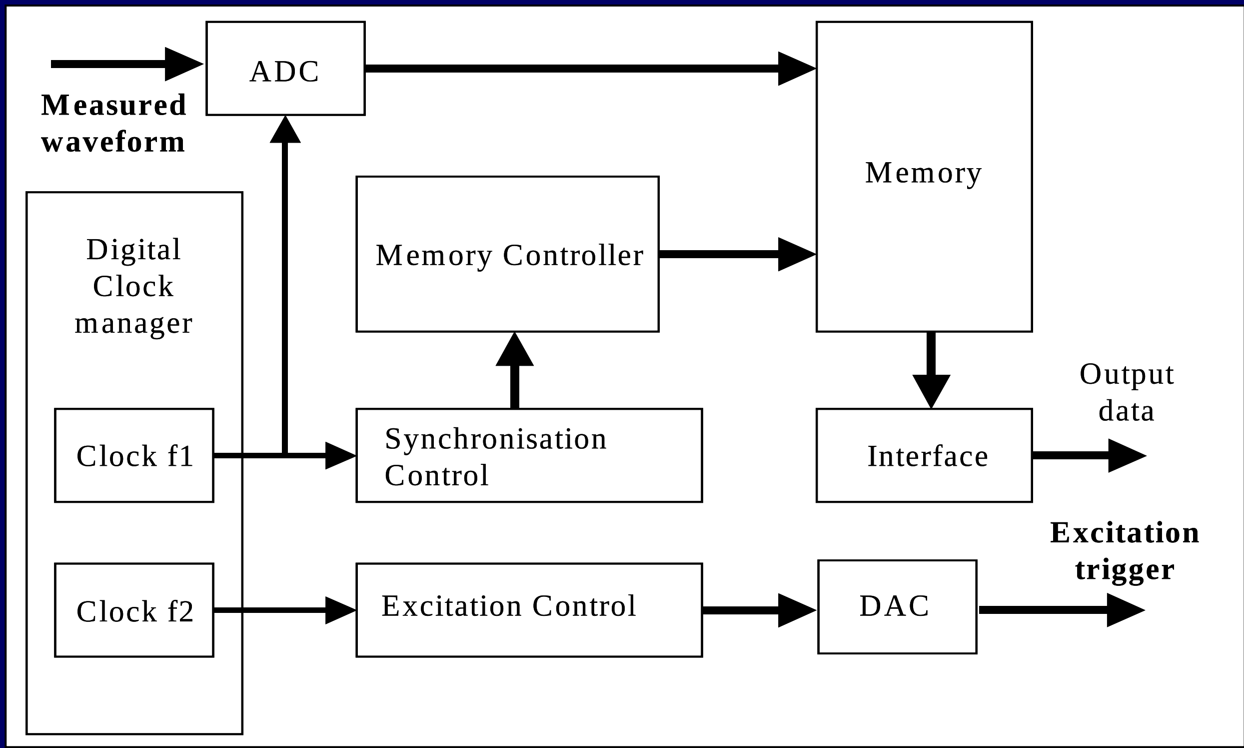
Accurate Interleaved Sampling



Operation of two clock architecture for the clock ratio 2:3 (dashed lines – excitation of a particular frame, dotted lines – sampling instants)

ASIC application and Background

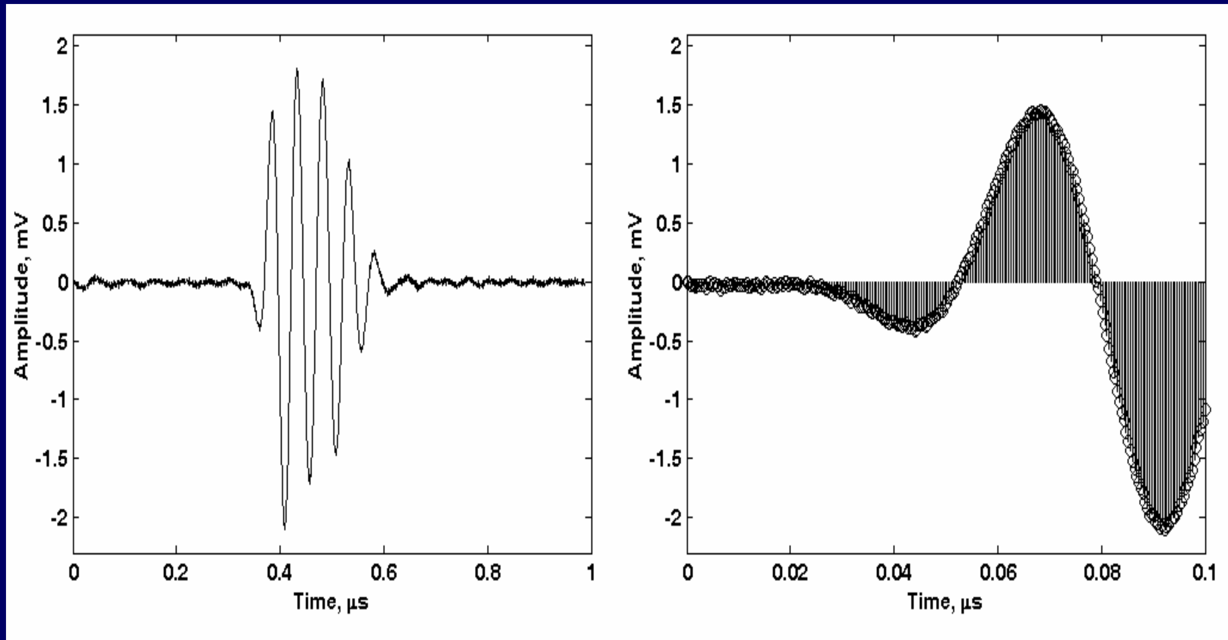
Accurate Interleaved Sampling



Block diagram of two clock timing architecture

ASIC application and Background

Accurate Interleaved Sampling



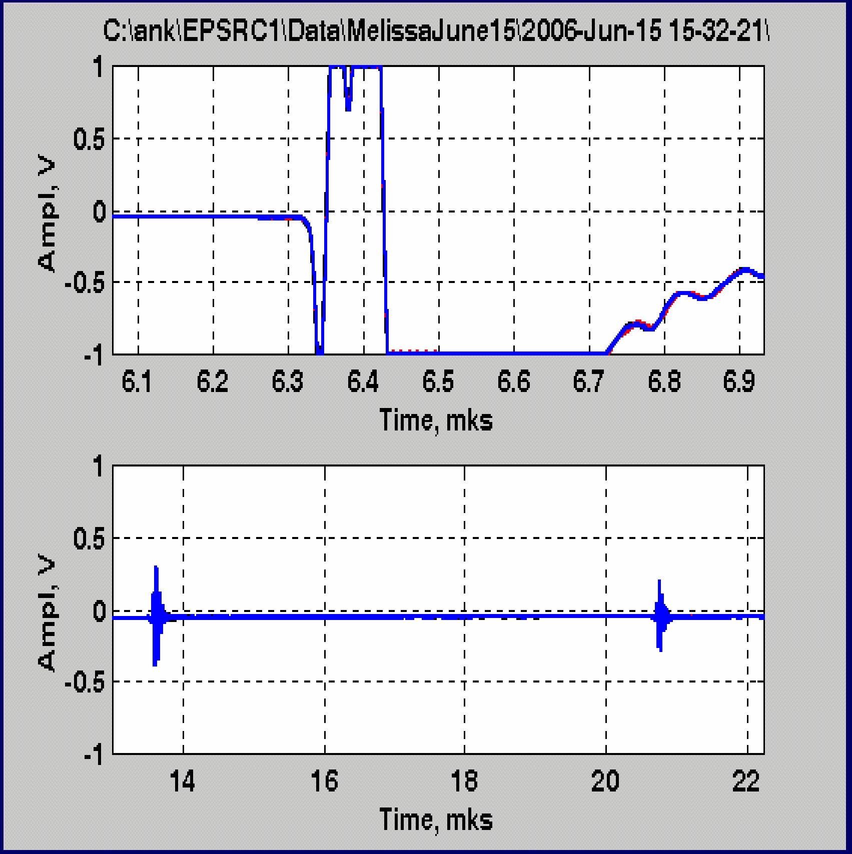
Experimentally recorded ultrasonic signal

(clock ratio 26/27, ADC frequency 80 MHz, equivalent sampling frequency 27*80=2160 MHz, 1024 averages, transducer central frequency 20 MHz)

ASIC application and Background

Main features implemented in new architecture:

Self-calibration



Use of two acquisition windows to capture both the excitation pulse and the response

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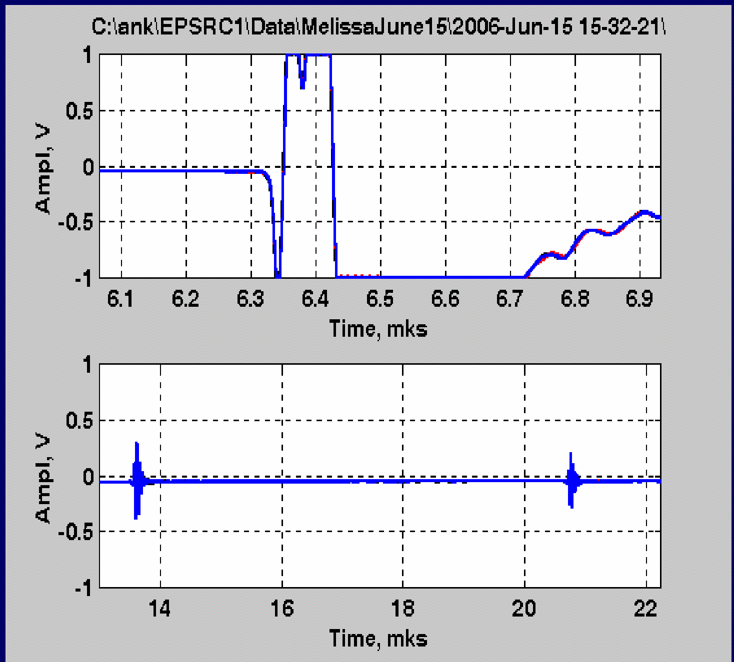
ASIC application and Background

Main features implemented in new architecture:

Self-calibration

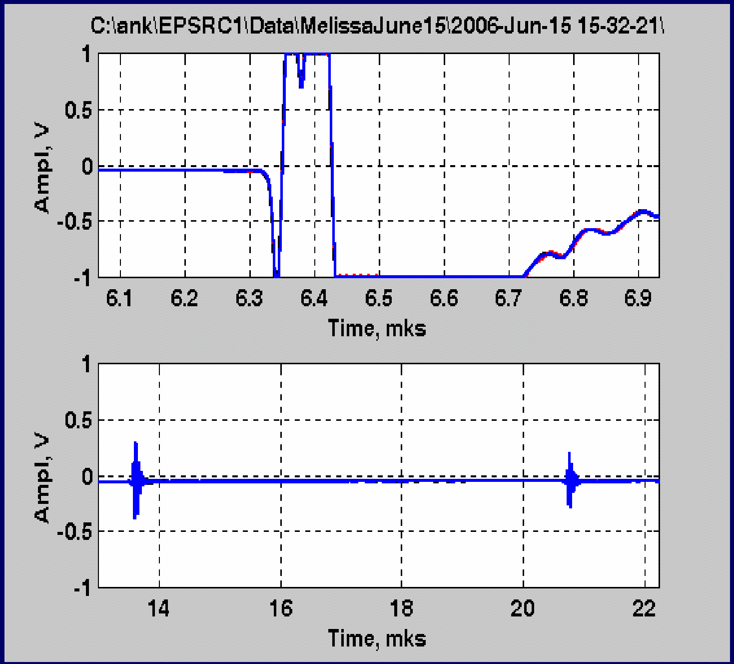


- First window is used for capturing the excitation pulse. Delay of pulse is affected by environmental influence on pulser's operation.
- The second window is used for capturing the response of the interrogated medium. The time difference between the two waveforms informs on the state of the medium.
- Elimination of the warming up influence allows monitoring with an accuracy improved by up to 10% in some experiments.

ASIC application and Background

Main features implemented in new architecture:

<u>Self-calibration</u>



- In case of medium with high attenuation an amplifier with adjustable gain should be used to provide commensurable values of both windows – this feature was implemented in ASIC2

ASIC application and Background

Main features implemented in new architecture:

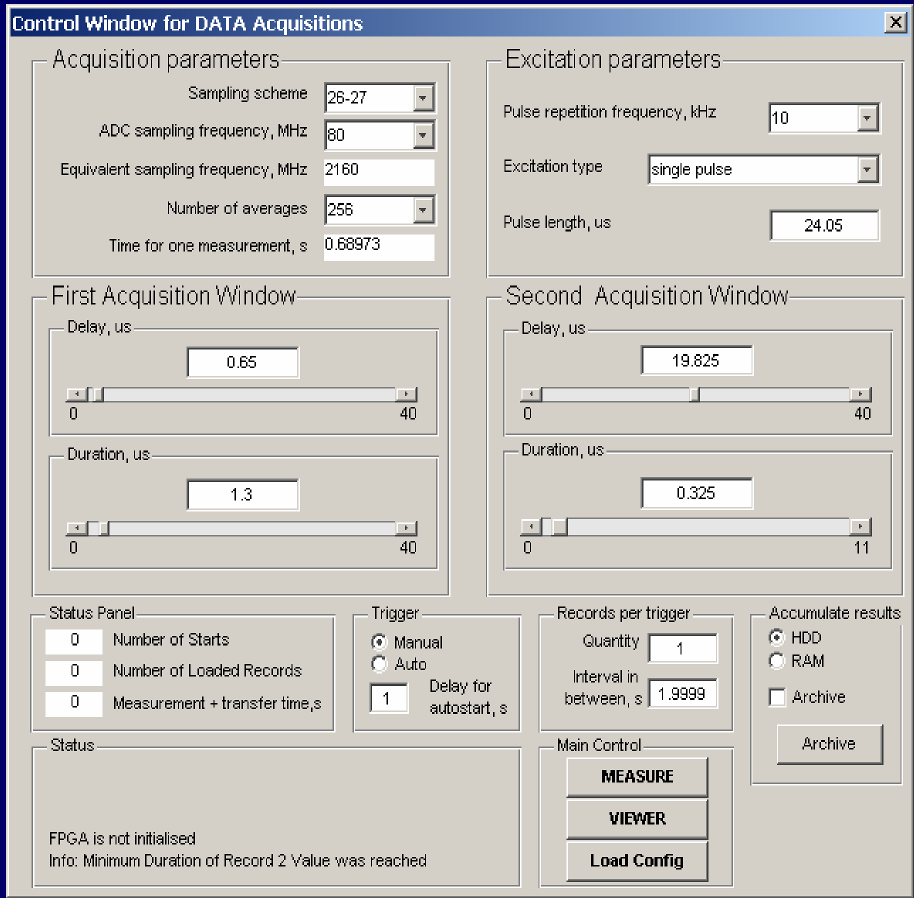
- Arbitrary function generator. This feature extents a set of attainable types of ultrasonic measurements.
- Mode compatible with Golay PRBS[1] excitation and appropriate acquisition followed by cross-correlation. This provides an additional to averaging SNR improvement and reduces measurement time.

[1] PRBS - Pseudo Random Binary Sequence

ASIC application and Background

Main features implemented in new architecture:

<u>Graphical User Interface</u>



GUI works in Matlab environment

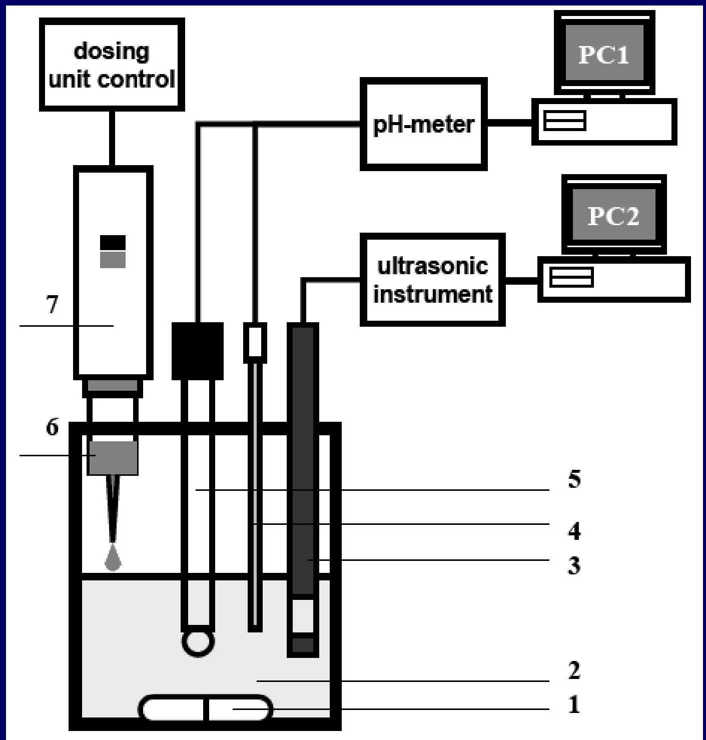
ASIC application and Background

Principal characteristics of implemented device

Sampling frequency	2.7 G samples/sec
Clock frequency	100 MHz
Frame length	35840 samples
Data width	32 bit
Flexible AFG feature	
Golay PRBS support	

Applications where the new instrument was involved

Super-resolution in situ ultrasonic monitoring of chemical reactions [5, 6]



Schematic of the experimental set-up

1 – magnetic stirrer,

2 – test solution,

3 – ultrasonic probe,

4 – temperature probe,

5 – pH probe,

6 – tip of the dosing unit,

7 – dosing unit

[5] K.L.Shafran, C.C.Perry, V.Ivchenko, R.E.Challis, A.K.Holmes and A.N.Kalashnikov, “Resolving complex chemical processes: comparison of monitoring by ultrasound with other measurement methods”, in Proc. 2006 IEEE Instrum. Measurem. Conf., 2006, pp.714-719.

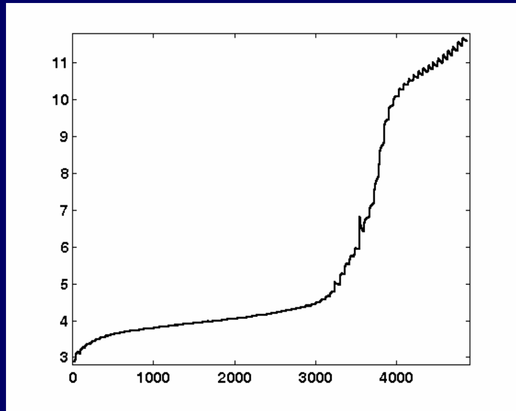
[6] A.N.Kalashnikov, K.L.Shafran, V.Ivchenko, R.E.Challis, C.C. Perry, “In situ ultrasonic monitoring of aluminium ion hydrolysis in aqueous solutions: instrumentation, techniques and comparisons to pH-metry”, accepted by IEEE Trans. on Instrumentation and Measurement on 12 April 2007 for publication in IMTC August 2007 special issue (IM-6277)

Applications where the new instrument was involved

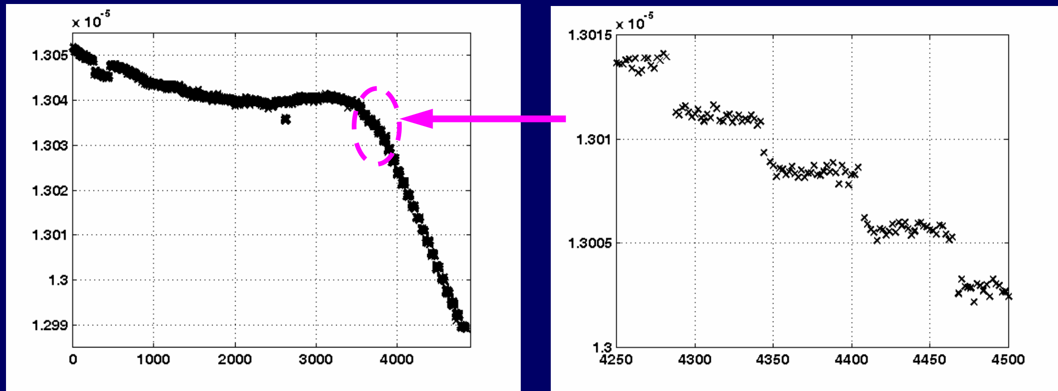
Super-resolution in situ ultrasonic monitoring of chemical reactions

Titration experiment ingredients

No	Sample	Titrant, its concentration (M) and volume of a single drop	Number of drops, time interval in between, change in ppm
1	HCl 0.169 M 100 mL	$AlCl_3$ 0.635 M 0.4 mL	60 30 s **300 ppm**
2	$AlCl_3$ 0.1156 M 100 mL	KOH 2.863 M 0.2 mL	80 60 s **210 ppm**



pH titration curve for the experiment 2



Ultrasonic titration curve for the experiment 2

Applications where the new instrument was involved

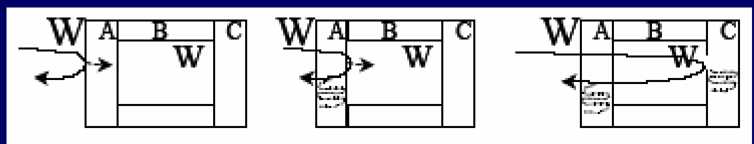
Super-resolution in situ ultrasonic monitoring of chemical reactions

- Ultrasonic spectroscopy offers a much higher resolution in time domain and a faster detection of chemical changes than pH-metry.
- The use of time-resolved ultrasonic titrations also allows to measure the mixture stabilization time after each titrant addition. This is very difficult for pH-metric measurement due to quite significant time lag.
- Ability of ultrasonic velocity measurements to detect precisely the equivalence point in the neutralisation has been demonstrated. This allows for potential replacement of commonly used pH-metry with ultrasonic spectroscopy as a very robust and fast in situ method for fast monitoring of similar processes.

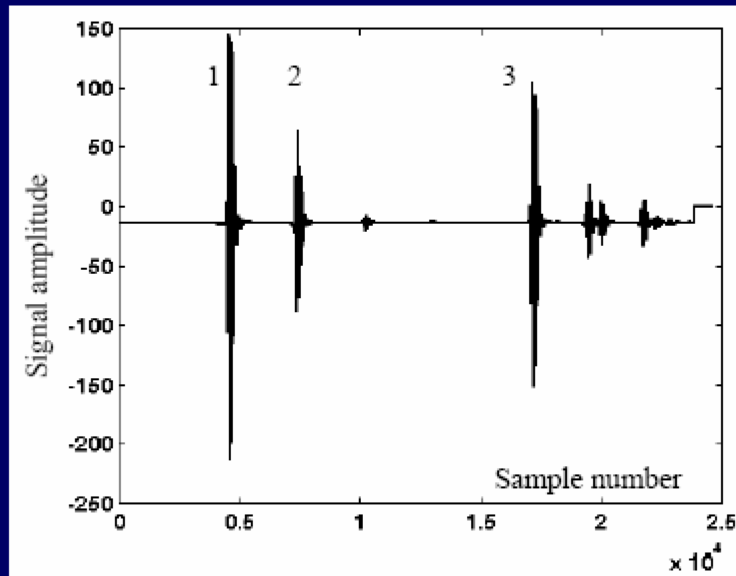
Applications where the new instrument was involved

Compensation for temperature variation in ultrasonic chemical process monitoring [7]

REFLECTOR WITH INTEGRATED TEMPERATURE SENSING FUNCTION



Acoustic pathways for reflection from the front face (1,left), from the entrance of the cavity (2, centre) and from the rear face (3,right)

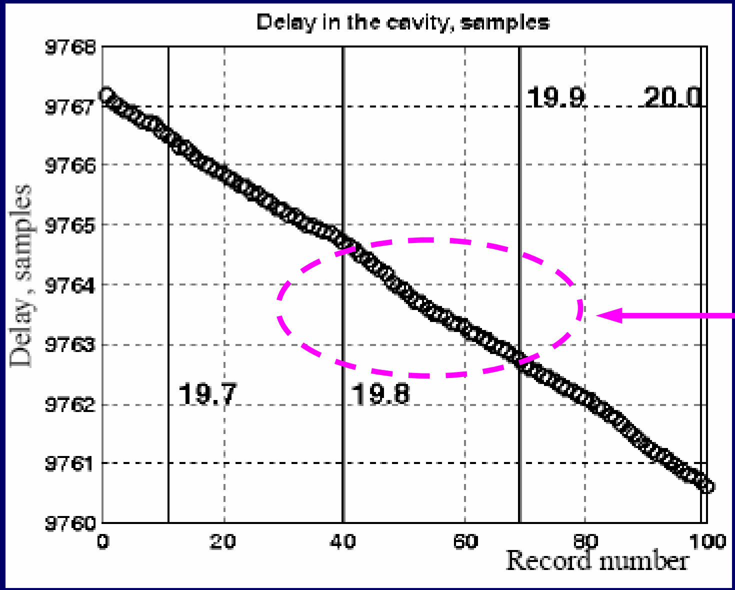


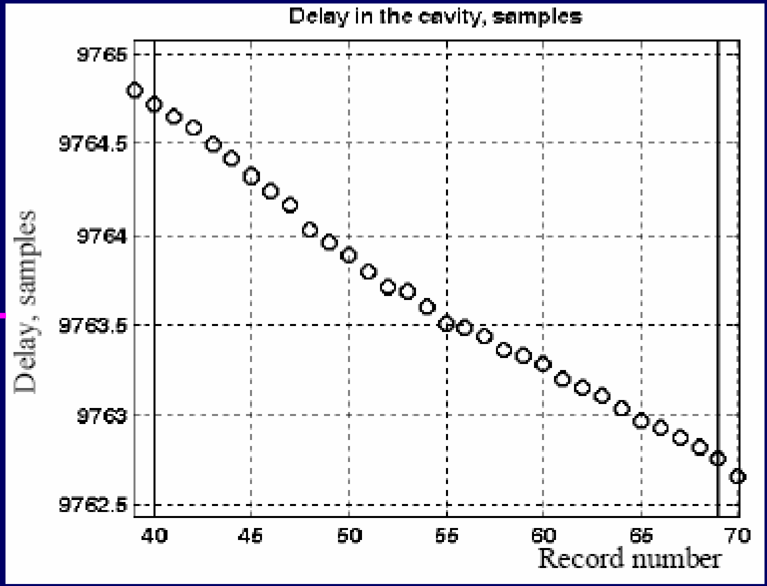
A signal recorded from the reflector with a water filled cavity, digits indicate contributions from the separate acoustic pathways, subsequent reverberations are not labeled

[7] A. N. Kalashnikov, V. Ivchenko, R. E. Challis and A. K.Holmes, “Compensation for temperature variation in ultrasonic chemical process monitoring”, in Proc. 2005 IEEE Ultrason. Symp., 2005, pp.1151-1154.

Applications where the new instrument was involved

Compensation for temperature variation in ultrasonic chemical process monitoring



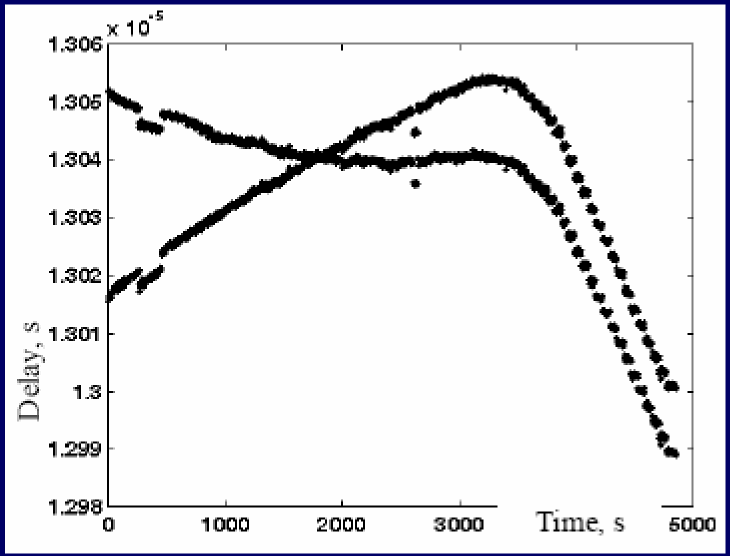


Estimated signal delays for 100 consecutive ultrasonic records (circles), vertical lines showing temperatures recorded using a conventional thermometer and their labels correspond to the temperatures, °C

Applications where the new instrument was involved

Compensation for temperature variation in ultrasonic chemical process monitoring

APPLICATION OF THE TEMPERATURE CORRECTION TO THE EXPERIMENTAL DATA



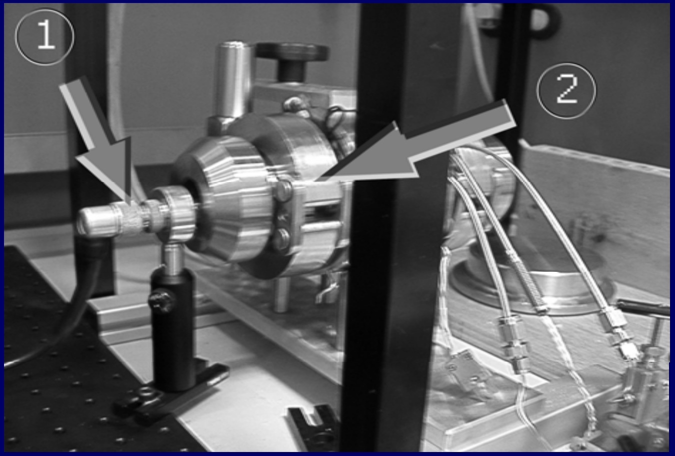
Experimental (from the upper left corner) and corrected delay curves

Corrected values show two almost linear slopes with different gradients.

This behavior is remarkably different from what can be observed from the raw data, and provides a much more useful insight into the formation of the precipitate in the reaction monitored.

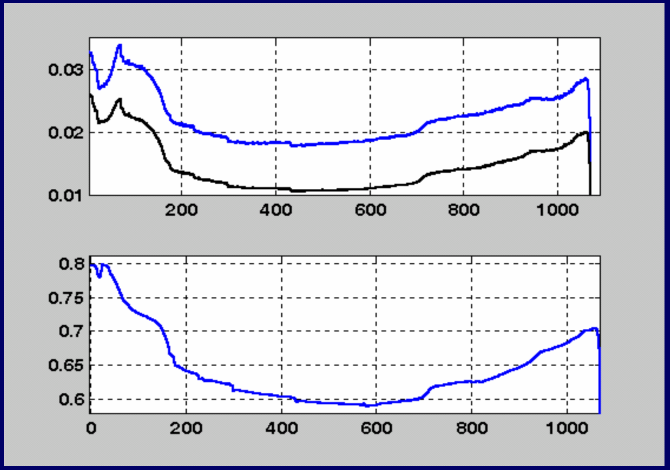
Applications where the new instrument was involved

In-process monitoring of foamed polymeric tissue scaffold fabrication [1]



Experimental setup for ultrasonic monitoring of a high pressure biological reactor;

1 - ultrasonic transducer,
2 - biological reactor



Scattered measured amplitudes of the single transit and triple transit signals (above), and smoother deduced reflection coefficient versus a number of a record acquired

[1] A. N. Kalashnikov, V.G. Ivchenko, R. E. Challis, W. Chen, “Self-calibrating scalable research platform for ultrasonic measurements in chemical and biological reactors”, in Proc. IEEE Instrum. Measurem. Conf., 2007

Applications where the new instrument was involved

In-process monitoring of foamed polymeric tissue scaffold fabrication

This application relates to production of bio-materials in high pressure bioreactors that were found difficult to monitor by optical techniques.

The fabrication process involved several phase transitions of the raw powder into a final air-bubbled bio-material through a liquid phase.

Measuring the reflection coefficient of the evolving medium contacting a sapphire window monitored these transitions in our initial experiments.

The measurements required high accuracy as the anticipated change in the reflection coefficient was rather small, and self-calibration was found essential as the acoustic contact between the window and the transducer pressed against it varied with variation of pressure in the reactor.

Graph shows the improvement in the curves when the reflection coefficient was self-calibrated by using the ultrasonic triple transit signal.

Available application fields

Any measurements with repetitive nature and where high timing resolution is crucial:

- High spatial resolution ultrasound imaging,
- Electronic devices parameterisation,
- Transmission lines testing, etc

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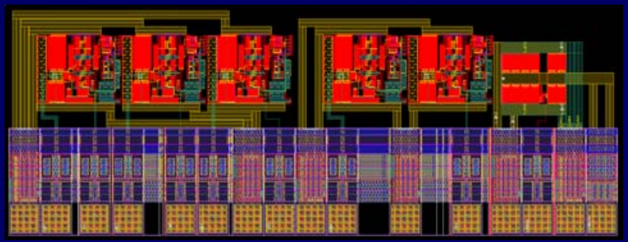
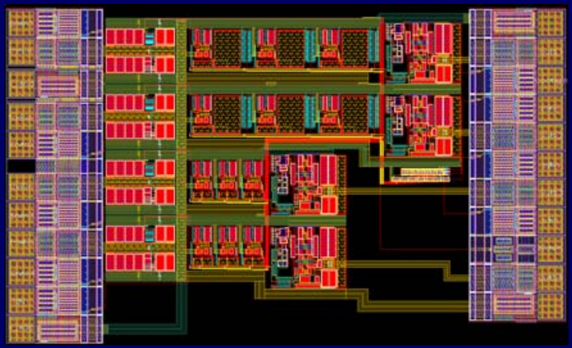
Chips design and layout aspects

Two ASIC designs were implemented:

ASIC1 - to develop and test of electronic components for an integrated ultrasonic front end ASIC



ASIC2 - four-channel ASIC for an Integrated Ultrasonic Front End



Chips design and layout aspects

Requirements for components of ASIC1

Technology

ASIC is supposed to be used in advanced safety critical applications, so the low voltage technology was chosen - AMS C35B4C3 as providing necessary 3.3V I/O voltage and timing parameters

Chips design and layout aspects

Requirements for components of ASIC1

Design objectives for: Pulser

Operating parameters

Supply voltage	3.3 V
Rise/fall time	20 ns
Typical load	2 nF
Loading transducer central frequency	10-15 MHz
High output impedance when inactive	

Chips design and layout aspects

Requirements for components of ASIC1

Design objectives for: Amplifier

Operating parameters

Supply voltage	3.3 V
Bandwidth	> 50 MHz
Gain	~20 dB
Input referred noise	23.7 $nV/Hz^{-1/2}$
Output should bias the same amplifier	

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Chips design and layout aspects

Requirements for components of ASIC1

Design objectives for: Amplifier

Operating parameters

Supply voltage	3.3 V
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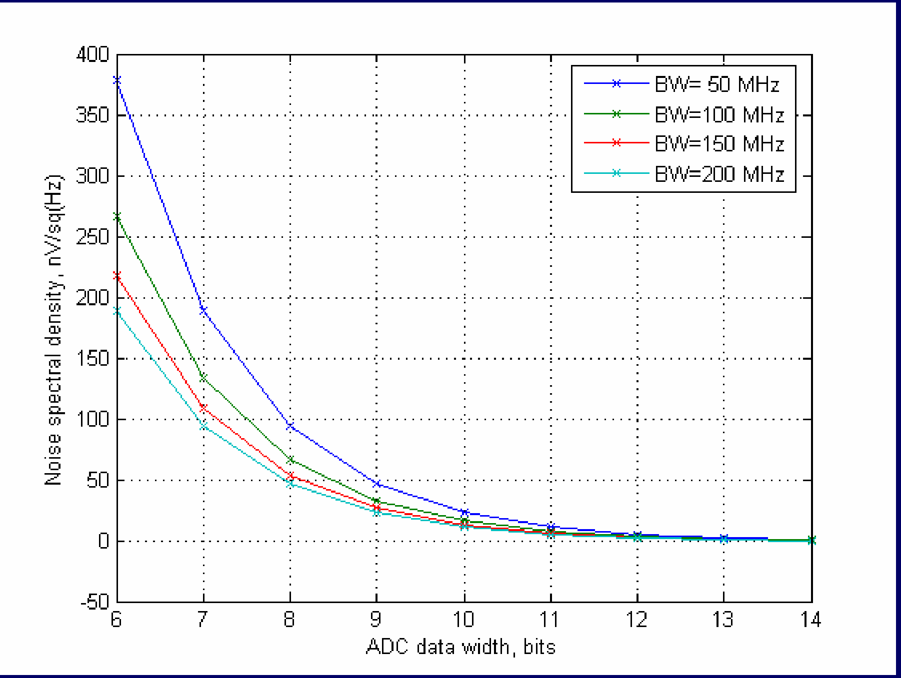
Chips design and layout aspects

Requirements for components of ASIC1

Design objectives for: Amplifier

Noise requirements evaluation

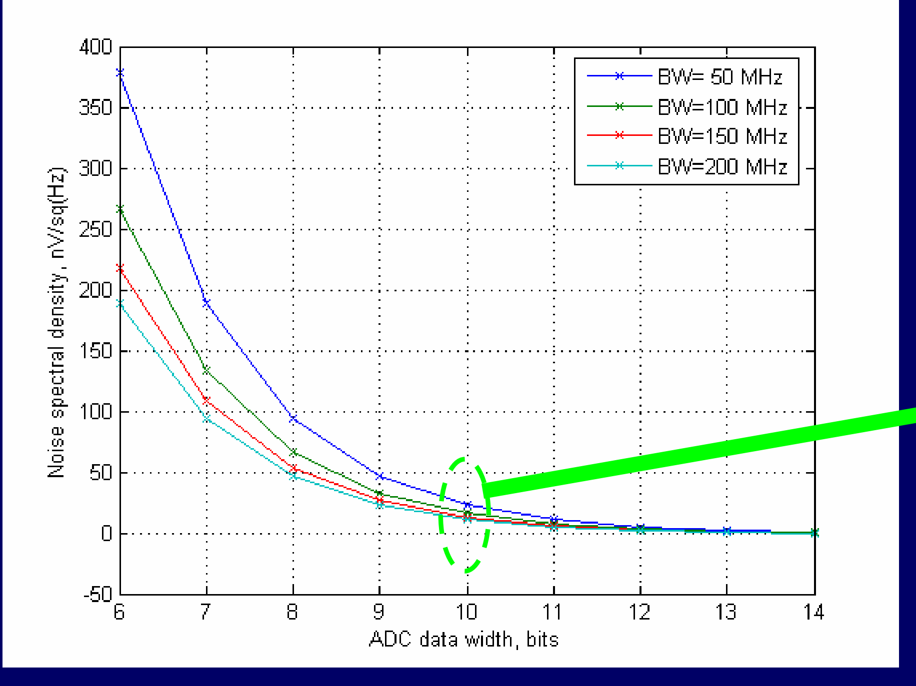


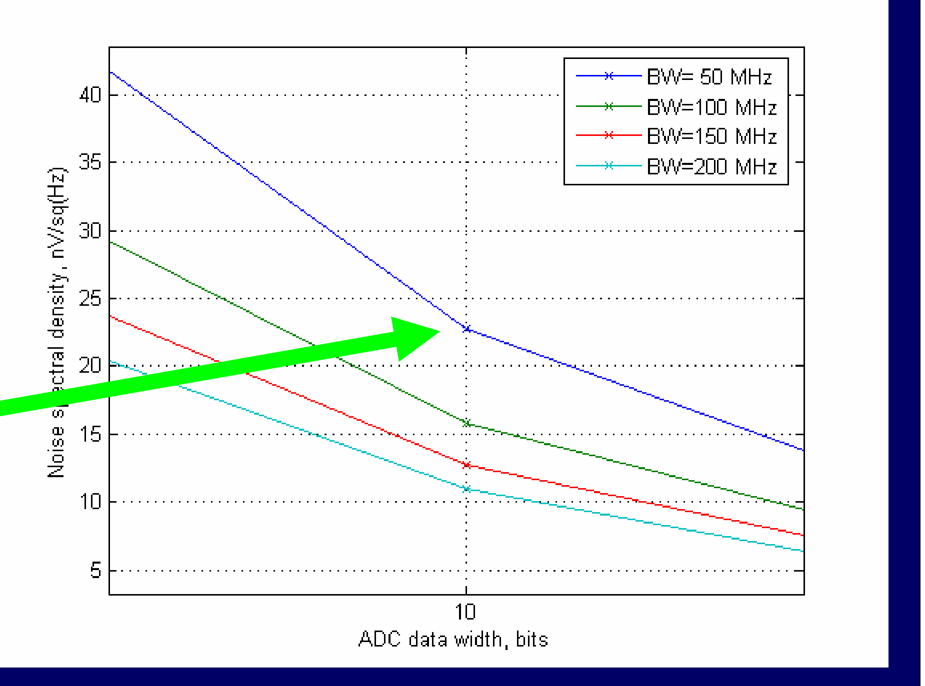
Chips design and layout aspects

Requirements for components of ASIC1

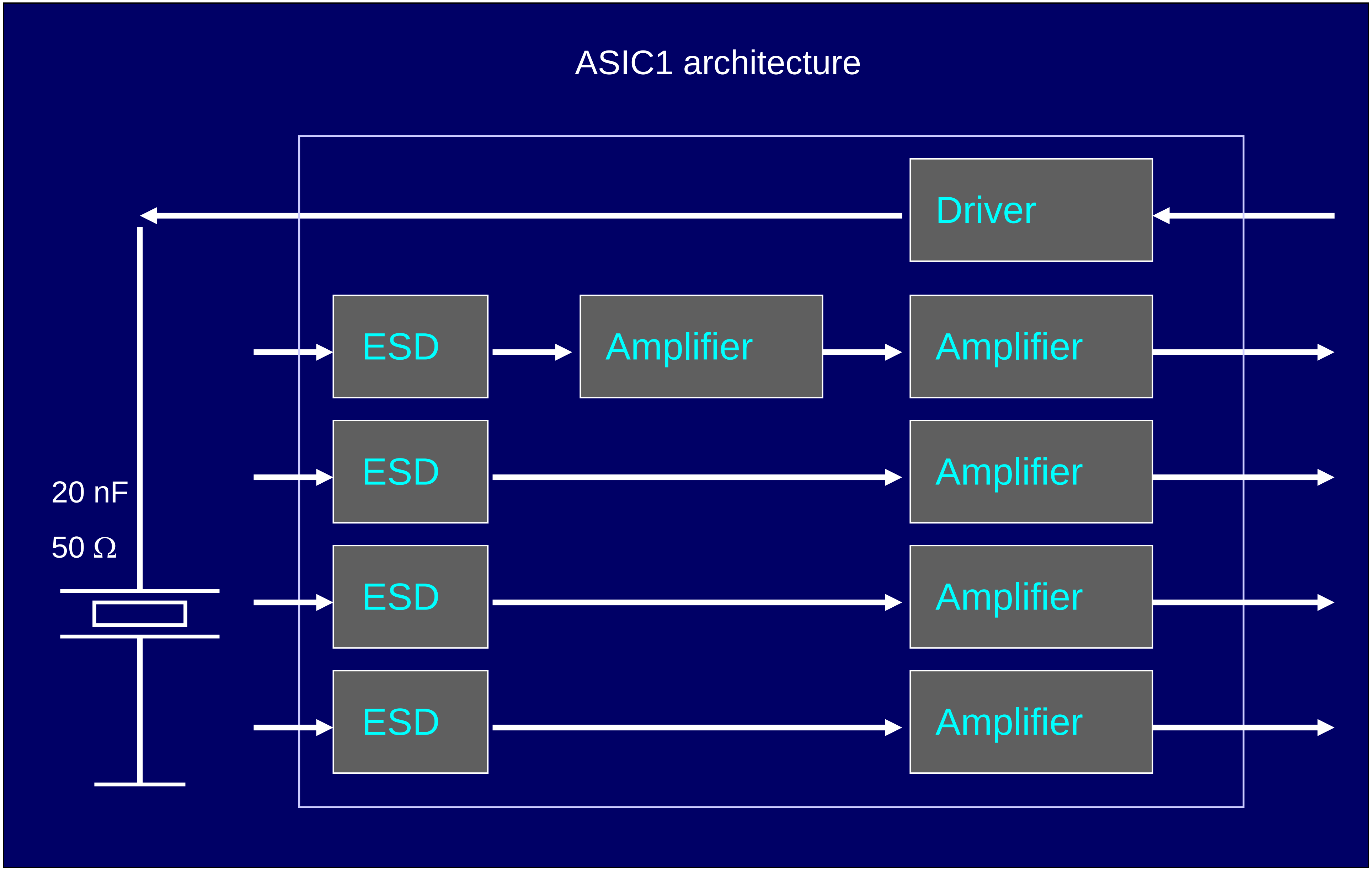
Design objectives for: Amplifier

Noise requirements evaluation





Chips design and layout aspects



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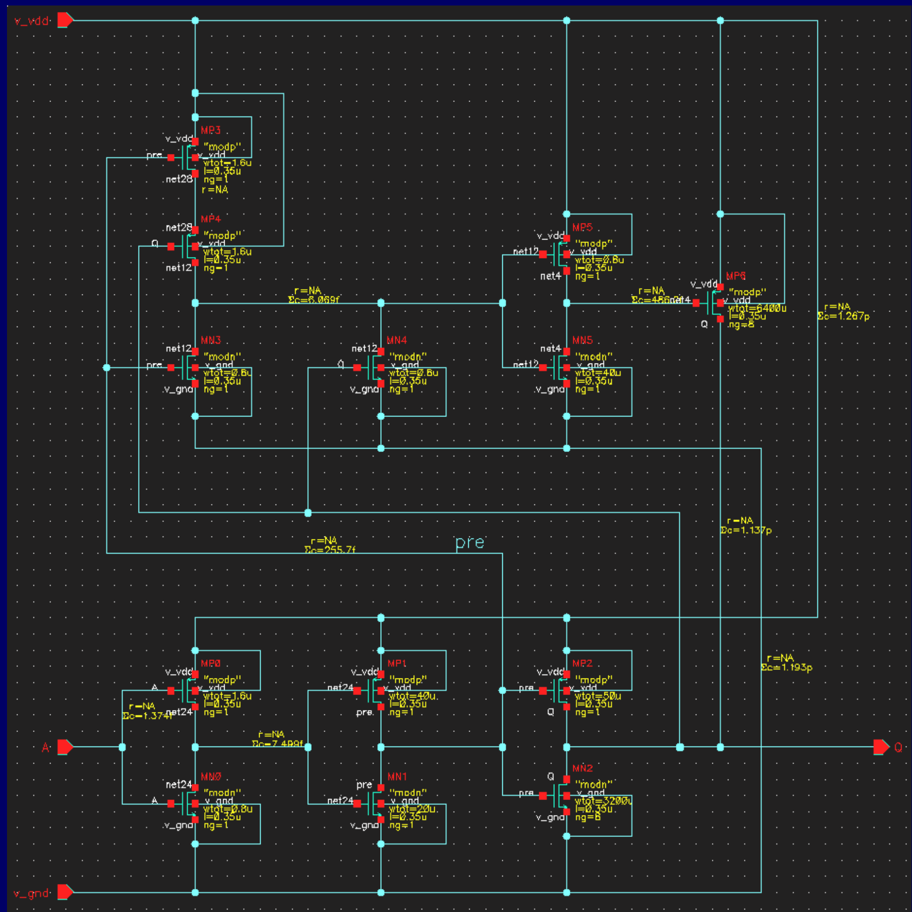
Chips design and layout aspects

Implementation of ASIC1

Pulser schematic [8]



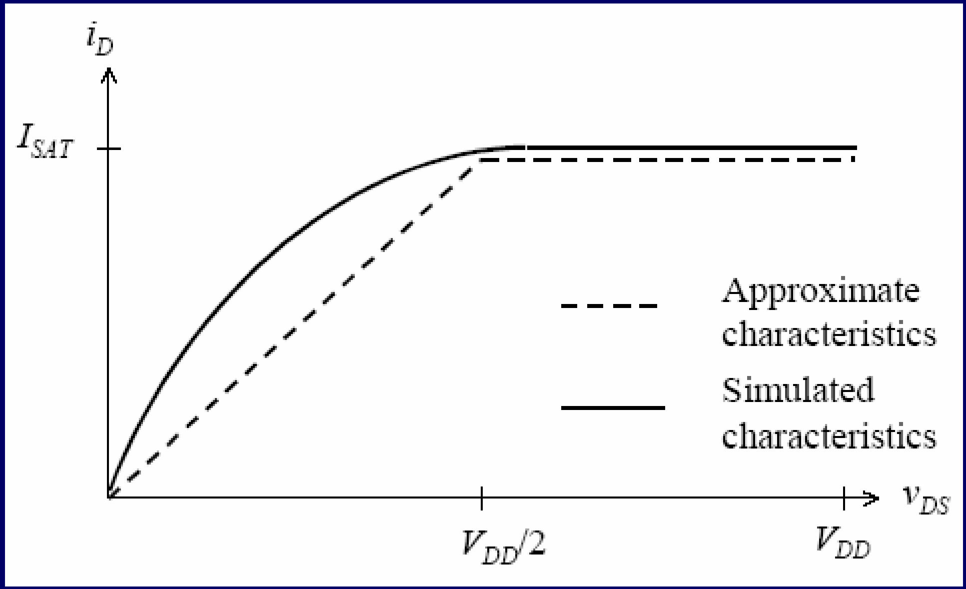
[8] J. Johansson, “Optimization of a piezoelectric crystal driver stage using system simulations”, in Proc. IEEE Ultrason. Symp.,2000, pp. 1049-1054.

Chips design and layout aspects

Implementation of ASIC1

Sizing of pulser output

$$t_f = 1.65 \cdot \frac{C_0 \cdot V_{DD}}{I_{SAT}},$$



MOS 3.3V N-Channel Electrical Parameters

saturation current 0.35µm	IDS035N	450	540	630	µA/µm

MOS 3.3V P-Channel Electrical Parameters

saturation current 0.35µm	IDS035P	-180	-240	-300	µA/µm

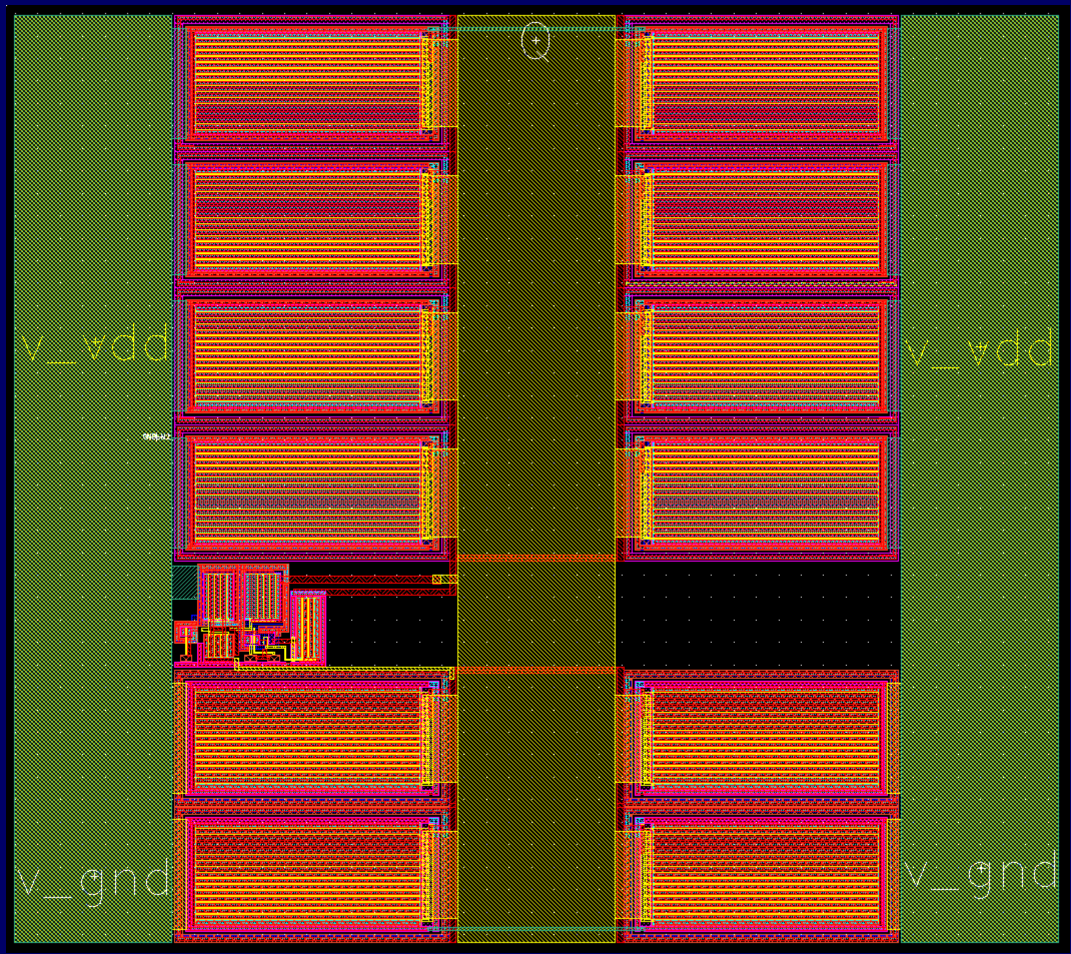
WN = 3200 µm

WP = 6400 µm

Chips design and layout aspects

Implementation of ASIC1

Pulser layout



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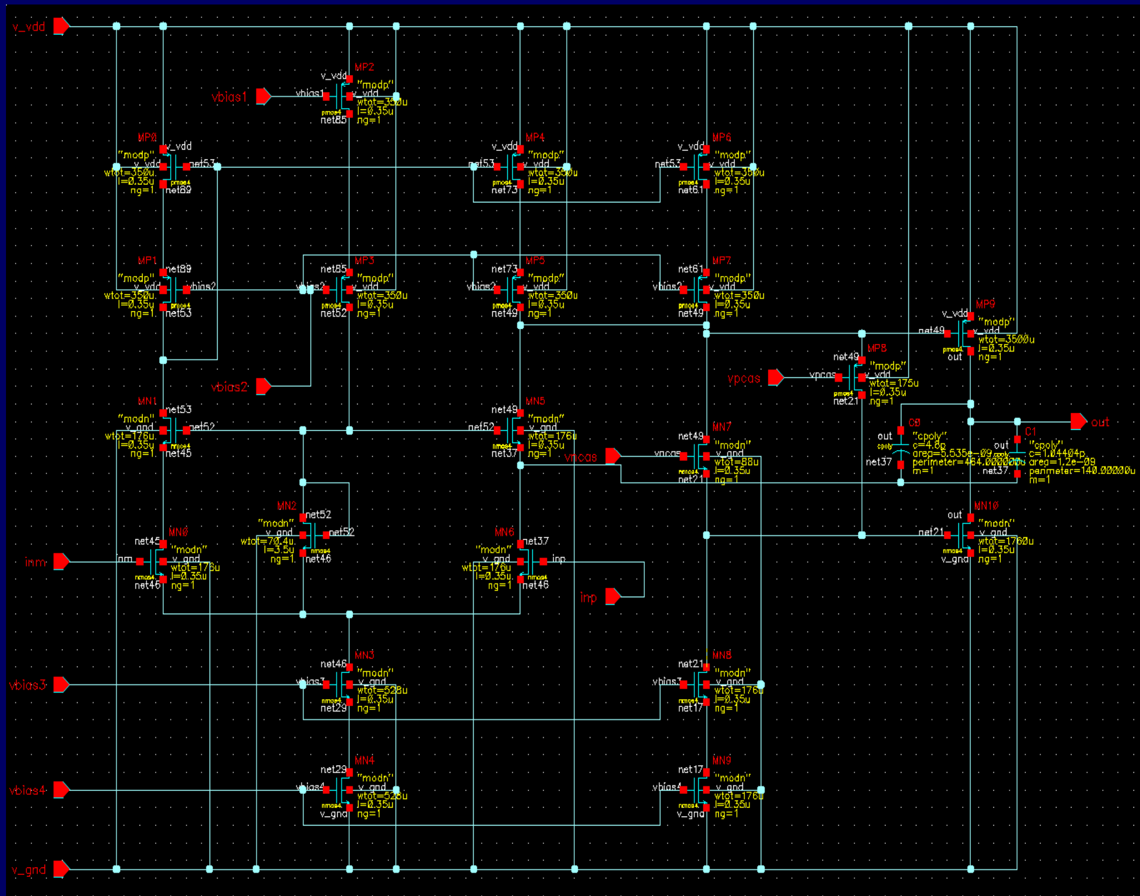
Chips design and layout aspects

Implementation of ASIC1

Amplifier schematic [9]



[9] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation, 2nd ed., Wiley, 2004, pp. 793-796.

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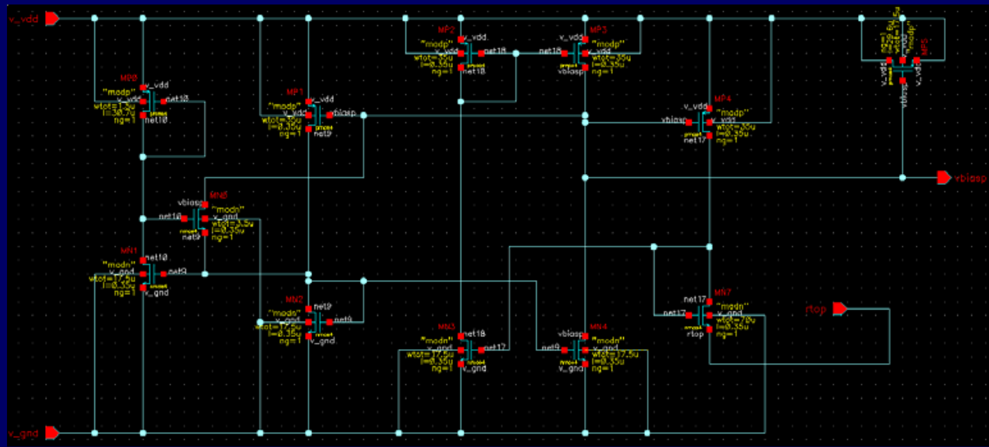
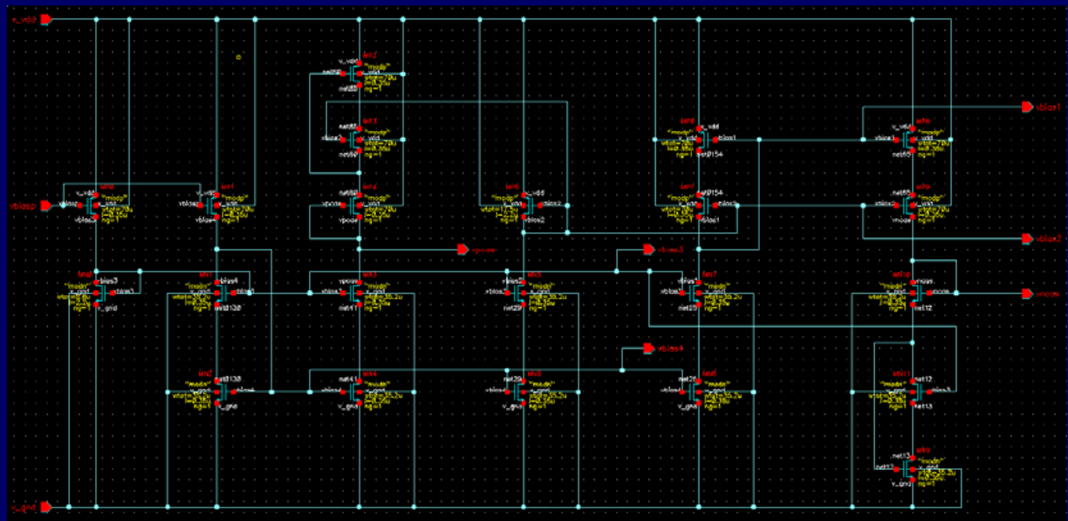
Chips design and layout aspects

Implementation of ASIC1

Bias circuits [10]



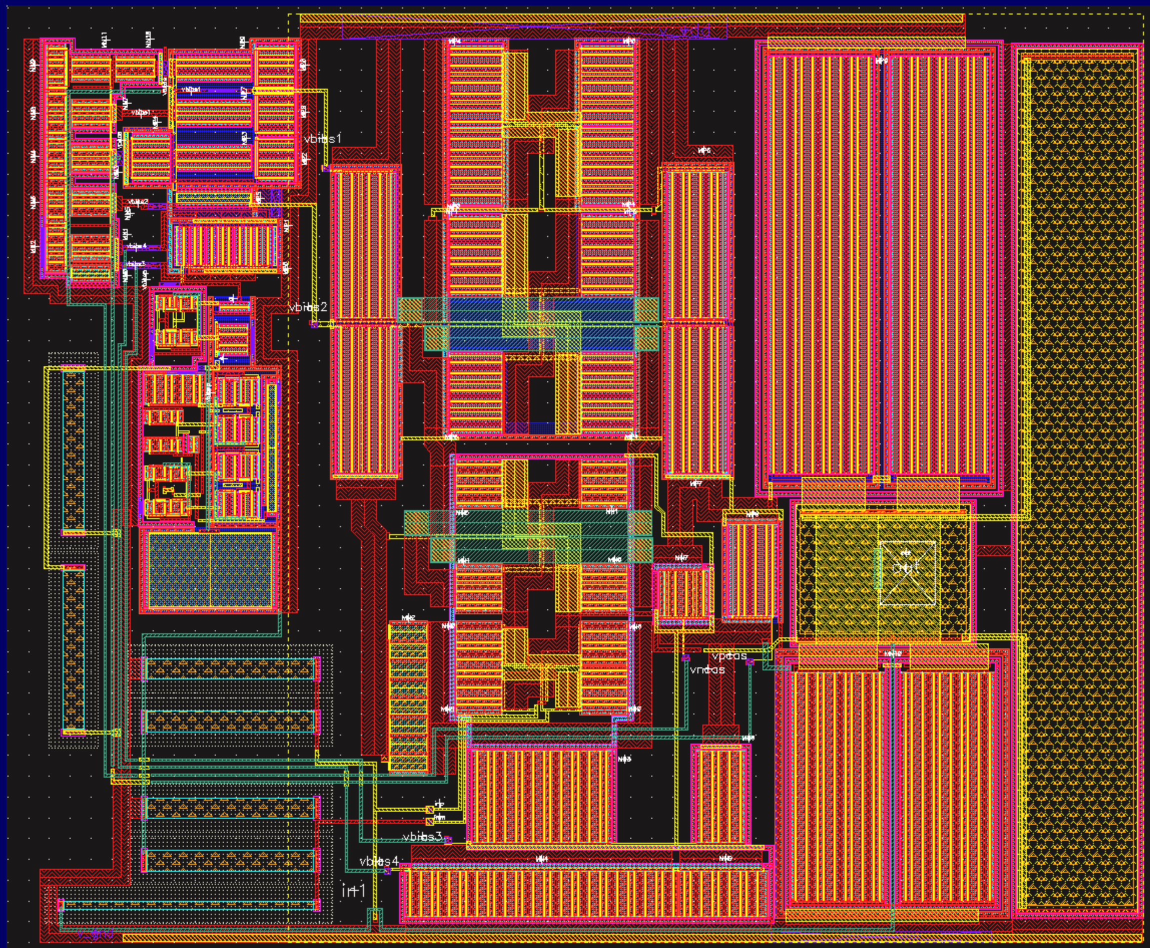


[10] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation, 2nd ed., Wiley, 2004, p. 650.

Chips design and layout aspects

Implementation of ASIC1

Amplifier layout together with bias circuit

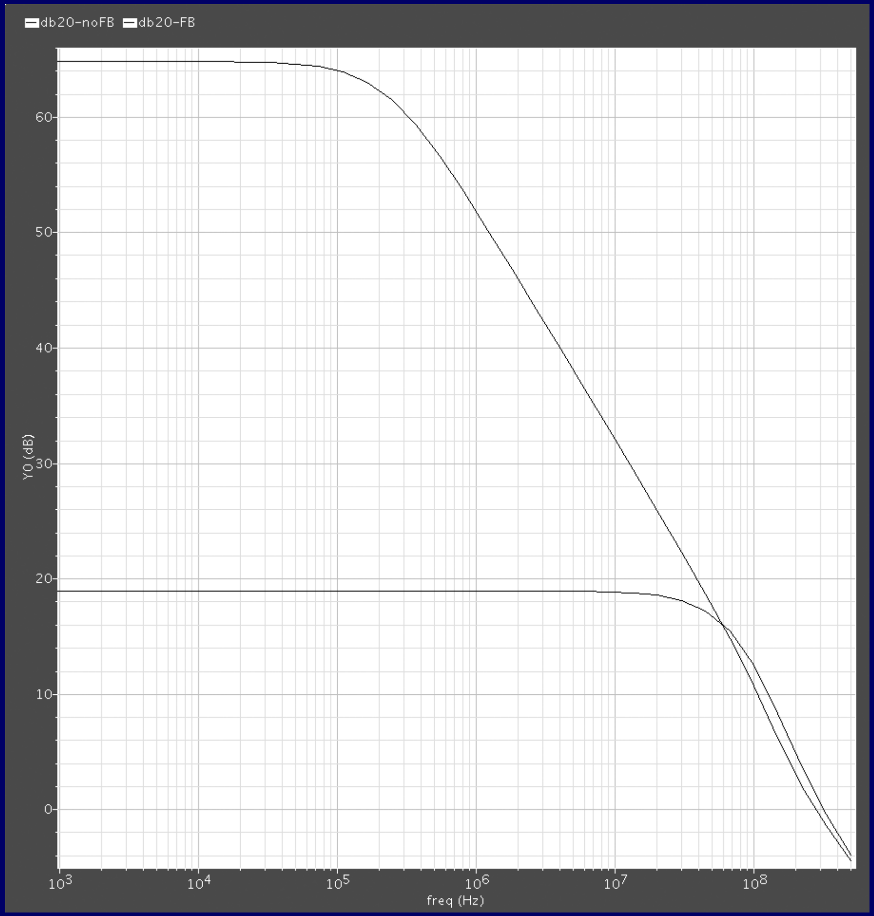


Chips design and layout aspects

Implementation of ASIC1

AC simulation of amplifier

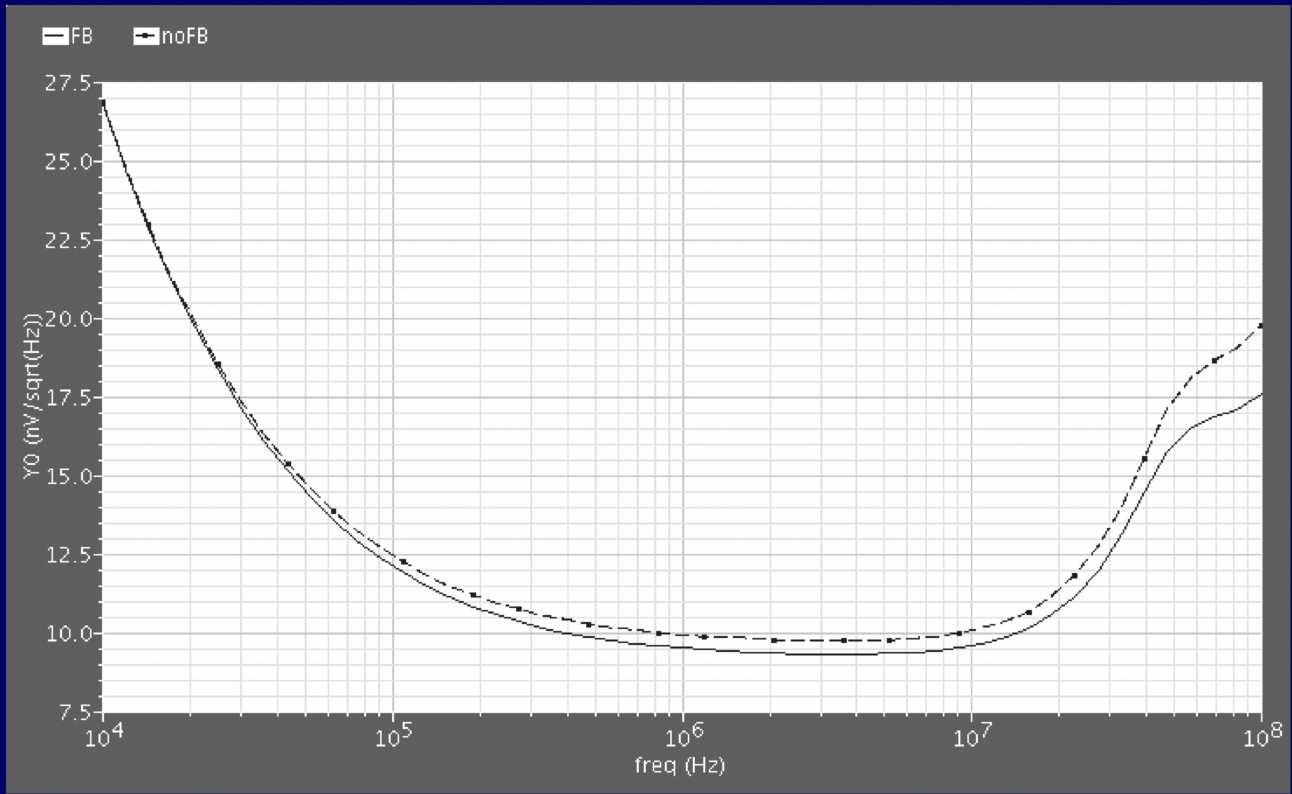
Load - capacitance 5 pF



Chips design and layout aspects

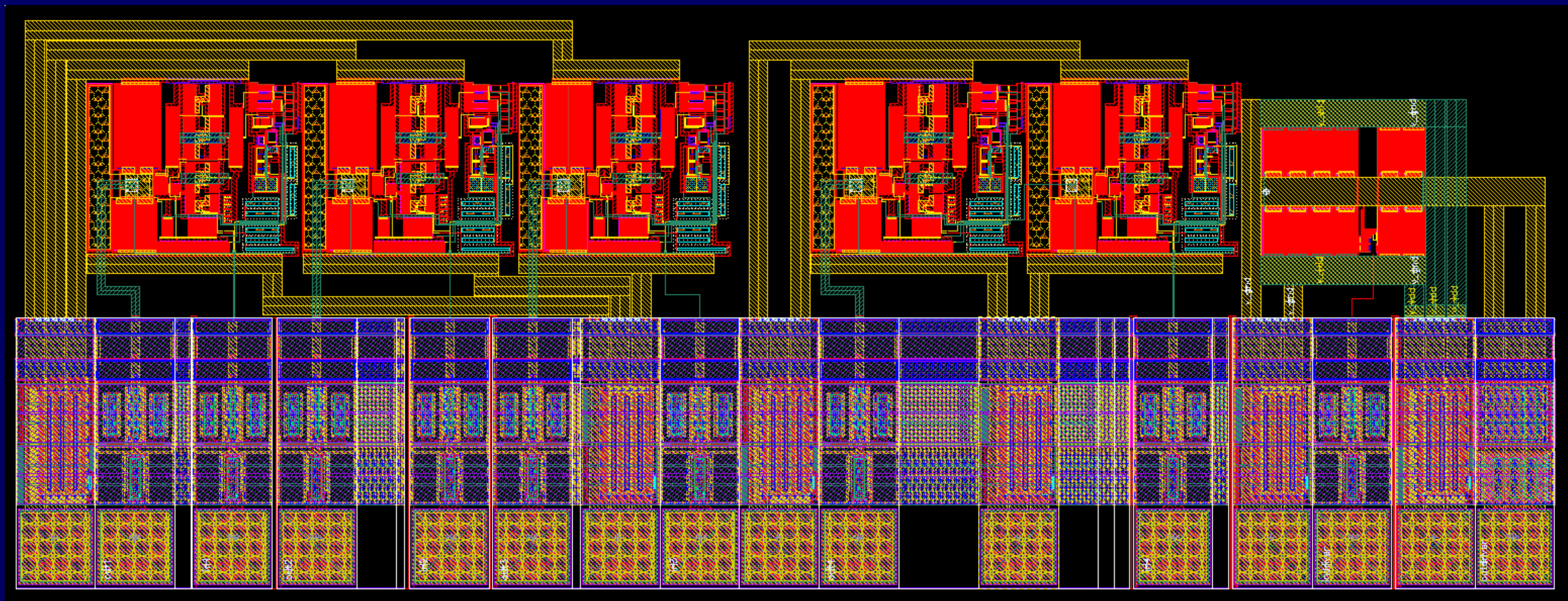
Implementation of ASIC1

Noise simulation of amplifier



Chips design and layout aspects

Layout of of ASIC1



Chips design and layout aspects

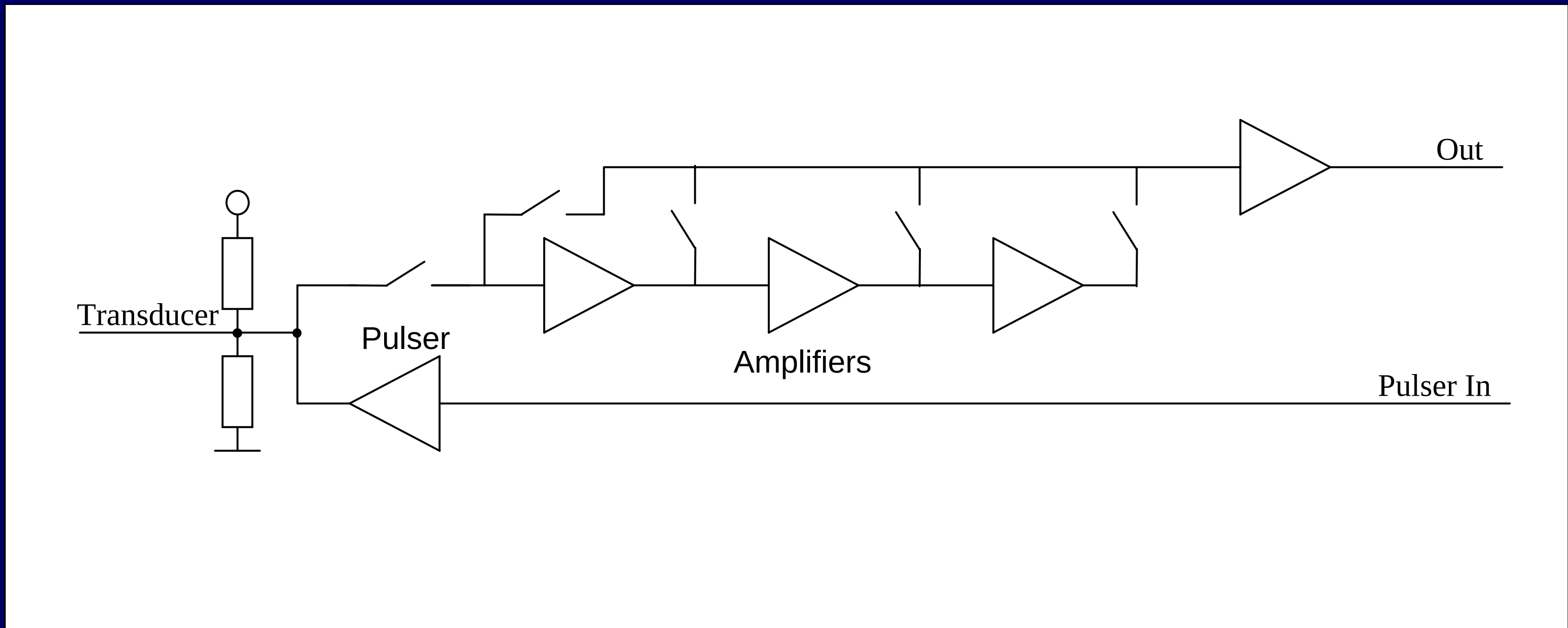
Design objectives for ASIC2

- Four channel design aimed for ultrasonic imaging of chemical processes
- Pulser and amplifier - same objectives as for ASIC1
- Compact protection circuitry for receiver
- Digital control of the front end configuration
  - downloadable configuration
  - cascading of amplifiers to control the gain
  - signals routing

Chips design and layout aspects

Implementation of ASIC2

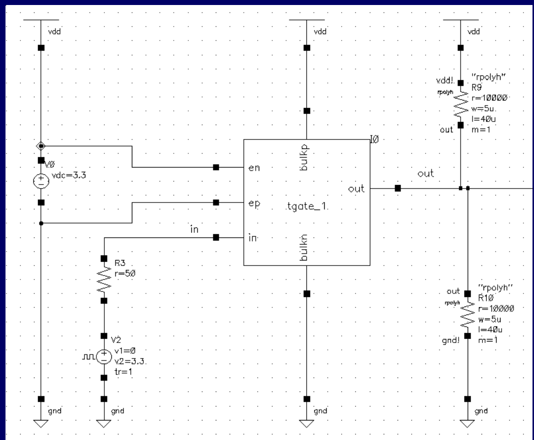
Structure of one channel

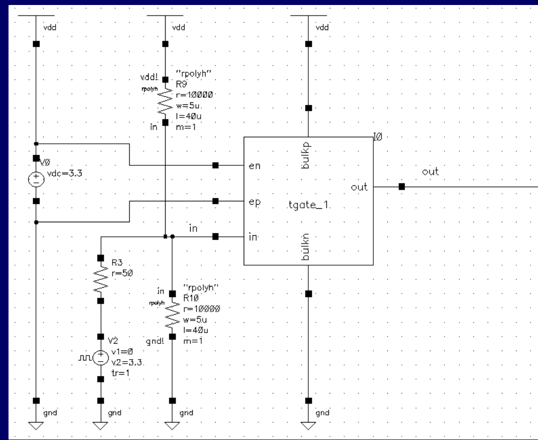


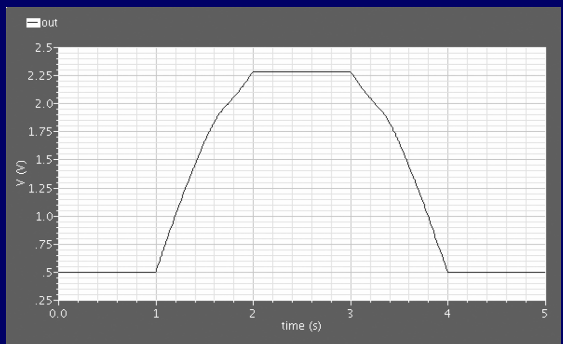
Chips design and layout aspects

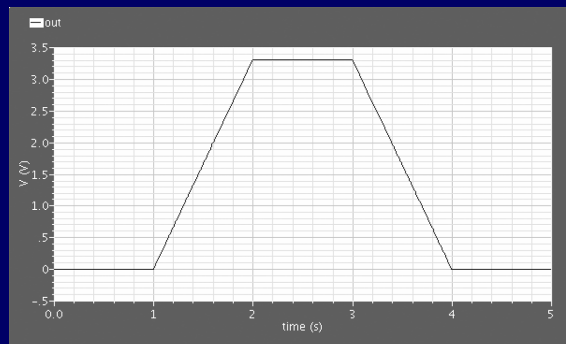
Implementation of ASIC2

Optimal location of transmission gate to provide linear transmission





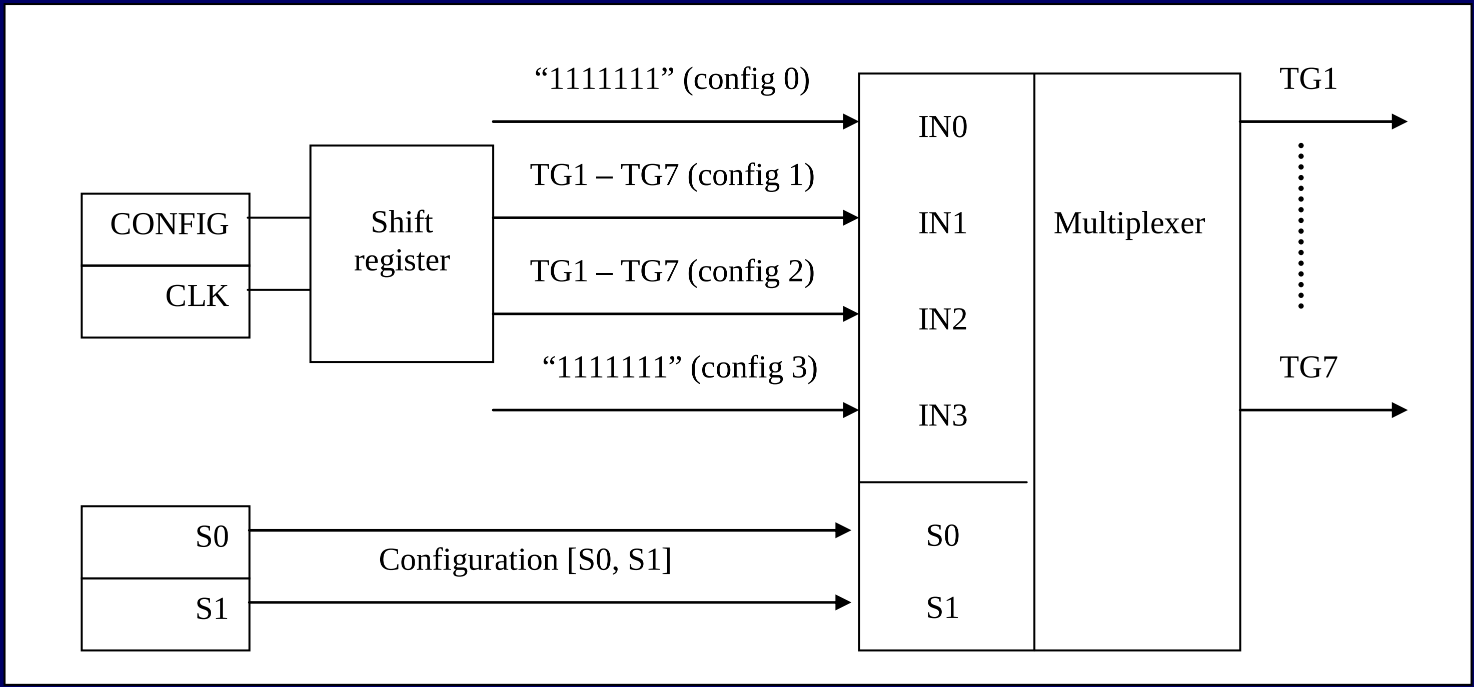




Chips design and layout aspects

Implementation of ASIC2

Digital control of the front-end configuration

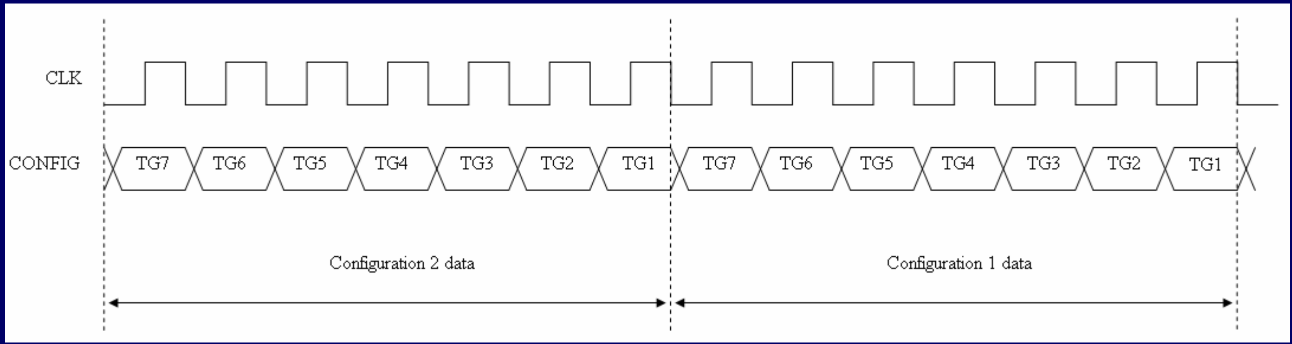


Load and switching of configuration schematic

Chips design and layout aspects

Implementation of ASIC2

Timing diagram of configuration loading



Selecting the configuration

S 0	S1	Multiplexer input connected	Configuration activated
0	0	IN1	Config 0
0	1	IN2	Config 1
1	0	IN3	Config 2
1	1	IN4	Config 3

Chips design and layout aspects

Implementation of ASIC2

Four operating modes (configurations) of the front-end

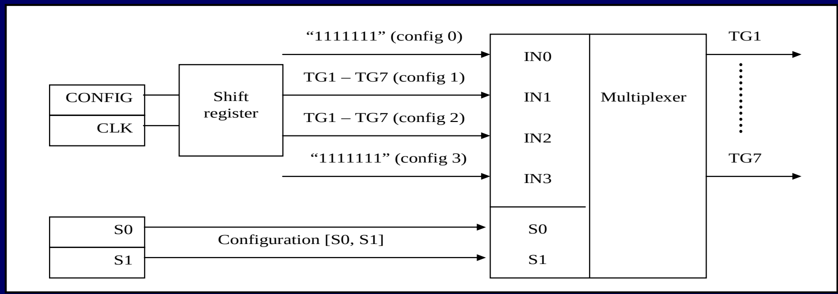
Configuration 0 – all transmission gates are closed

Configuration 1 – connections for 1st acquisition window (loaded in shift register)

Configuration 2 – connections for 2nd acquisition window (loaded in shift register)

Configuration 3 – driver drives, and all transmission gates are closed

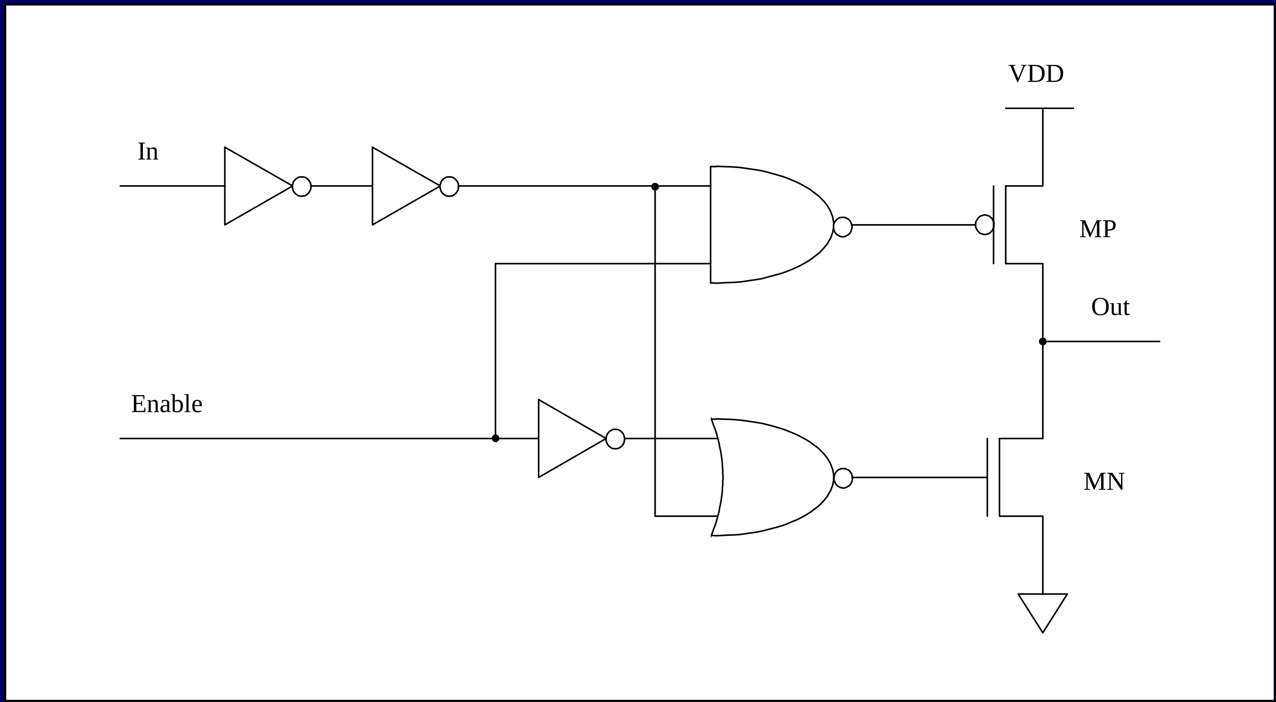
on-the-fly configuration handling - by manipulating of S0 and S1 inputs



Chips design and layout aspects

Implementation of ASIC2

Pulser: typical 3-state output schematic [11]



[11] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation, 2nd ed., Wiley, 2004, pp. 370-372.

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Chips design and layout aspects

Implementation of ASIC2

Pulser: typical 3-state output schematic

Disadvantages:

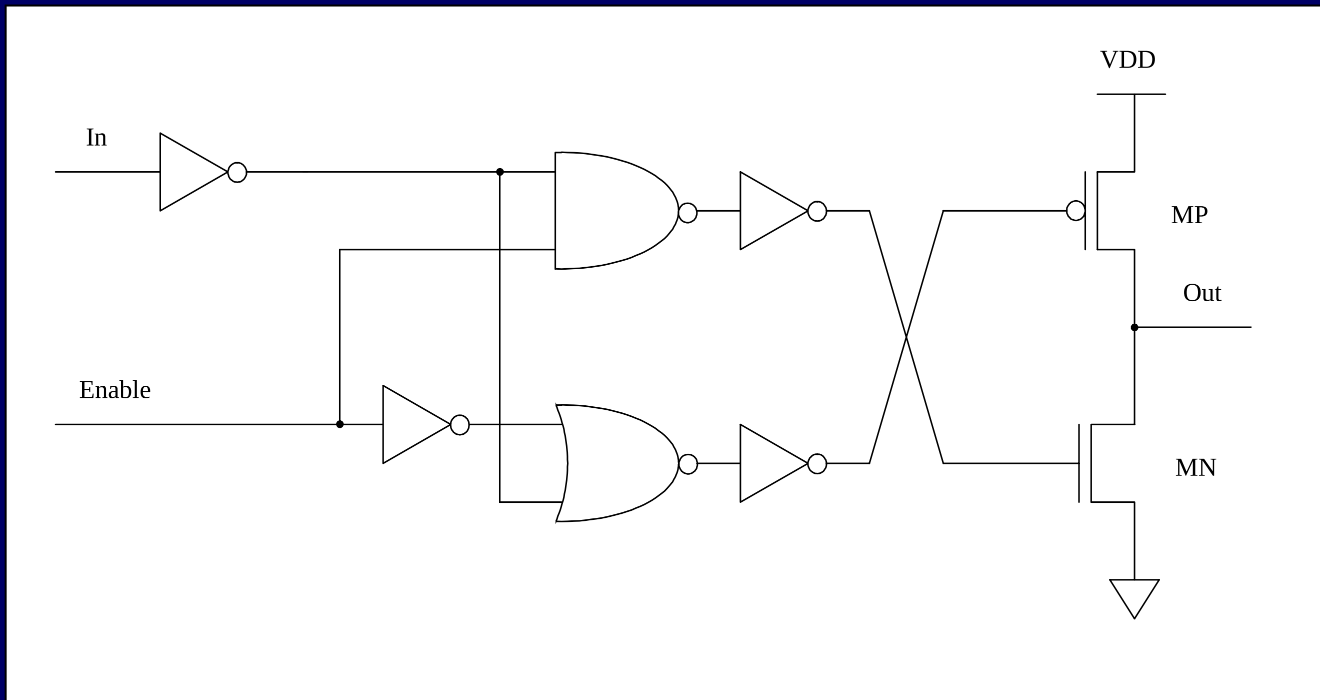
- NAND and NOR gates drive output stages and sense should be too large
- NAND and NOR gates should be increased twice as contain serial-connected transistors. This together with p.1 increases the topology’s space
- Asymmetry in NAND and NOR gates can deteriorate input signal of output stage.

To overcome these disadvantages second variant of pulser was implemented

Chips design and layout aspects

Implementation of ASIC2

Pulser: improved 3-state output schematic



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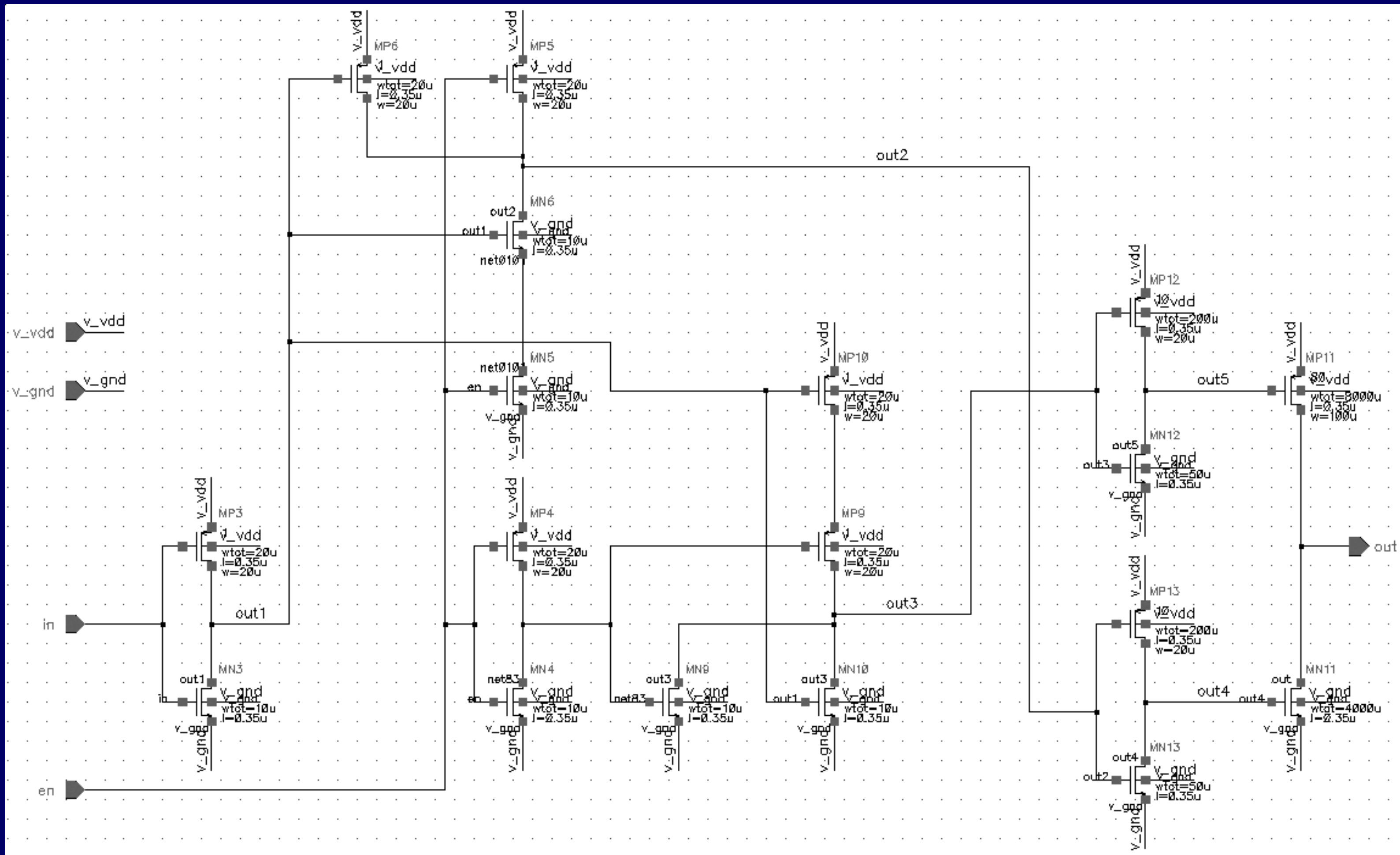
Chips design and layout aspects

Implementation of ASIC2

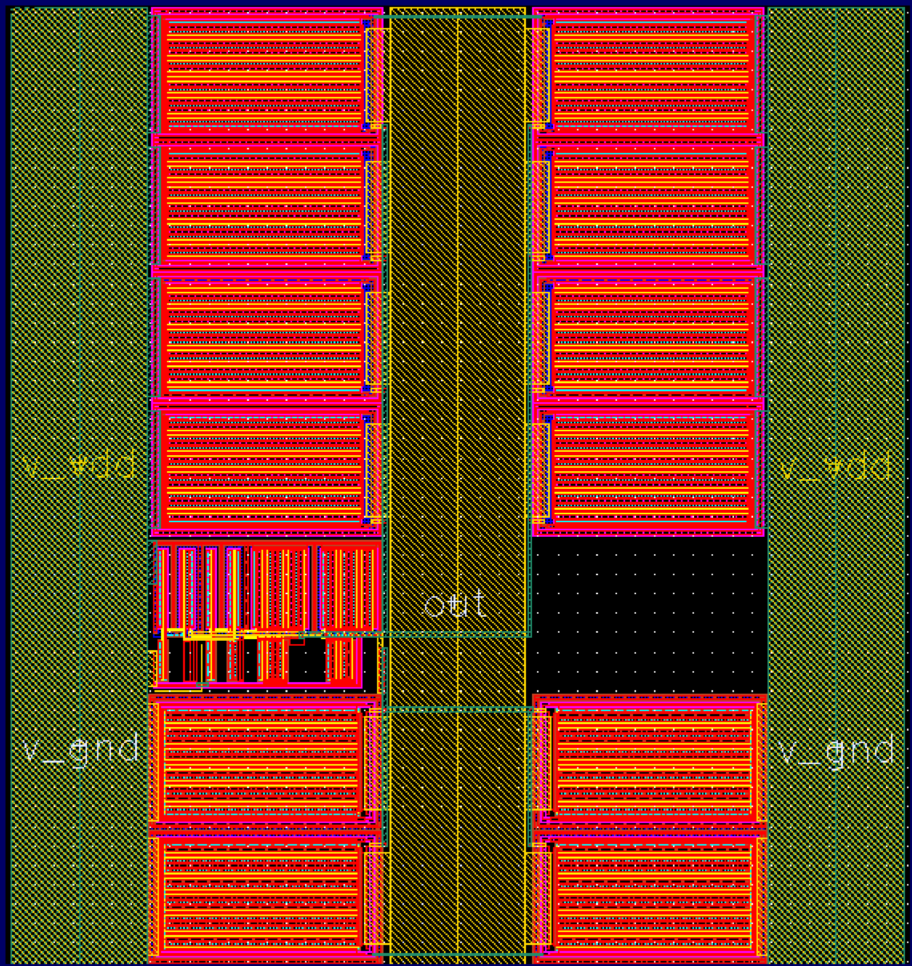
Pulser: improved 3-state output full schematic



Chips design and layout aspects

Implementation of ASIC2

Pulser layout



Chips design and layout aspects

Implementation of ASIC2

Amplifiers:

Two type of amplifiers were utilized:

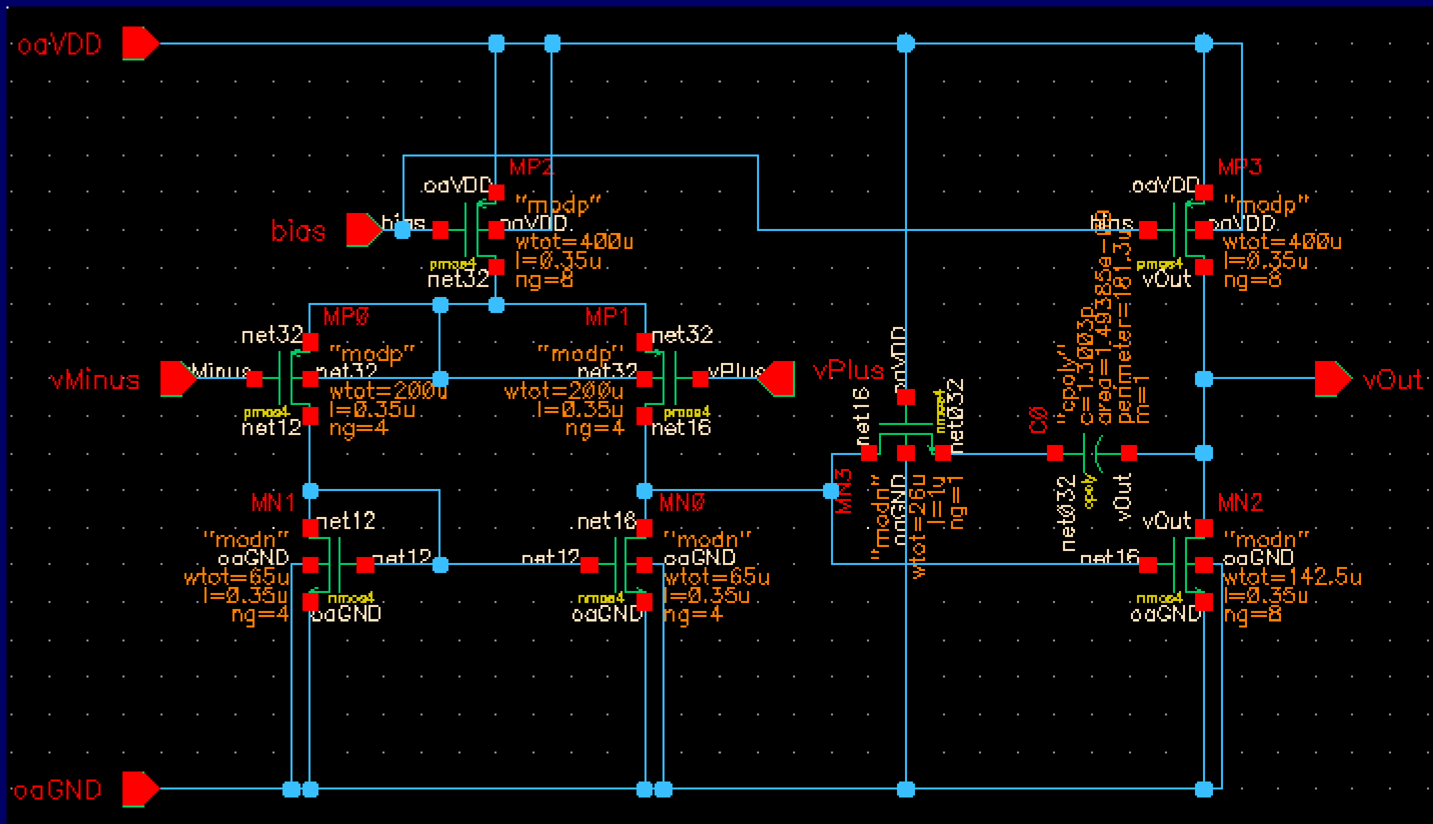
1) Amplifier prom previous ASIC1 design - it was used as output buffer

2) More compact low noise amplifier with p-channel transistors in differential pair

Chips design and layout aspects

Implementation of ASIC2

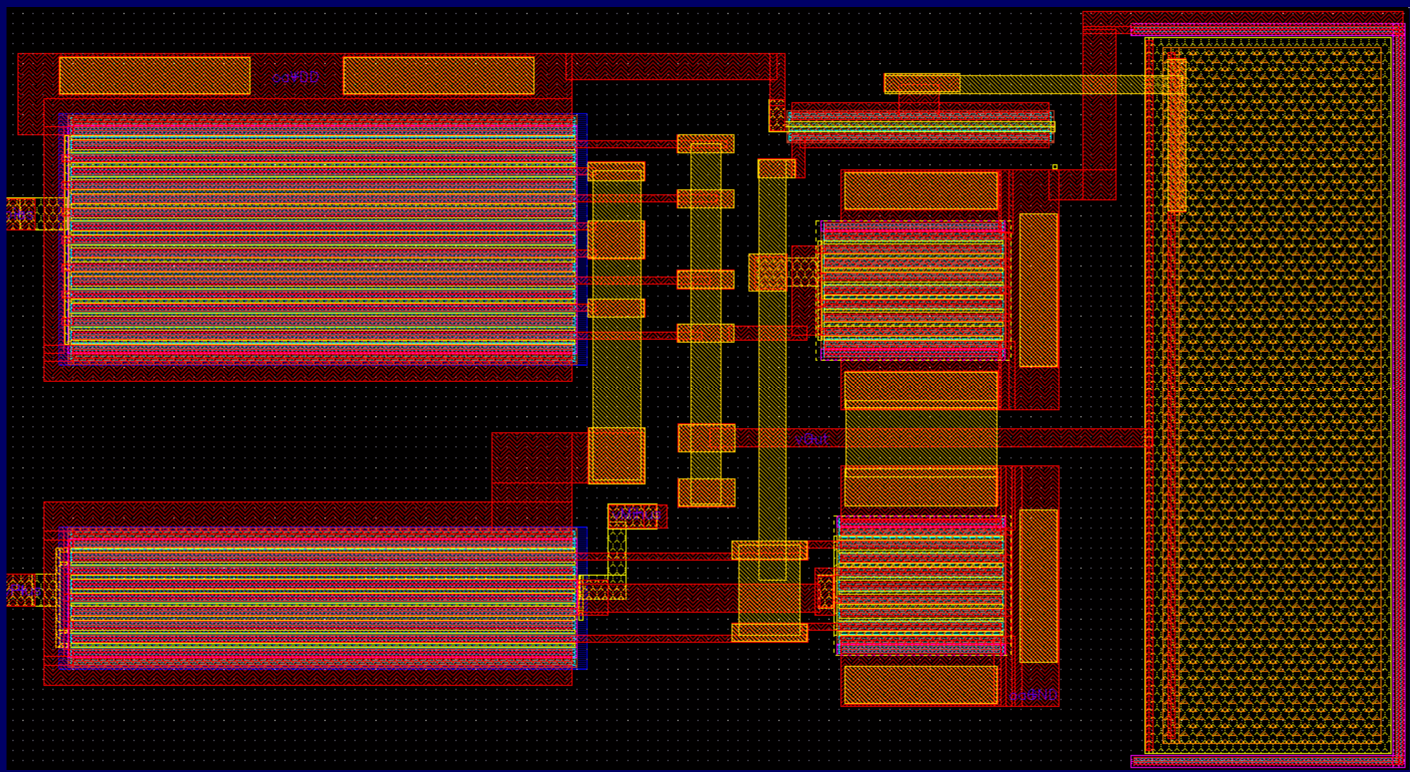
Compact amplifier schematic



Chips design and layout aspects

Implementation of ASIC2

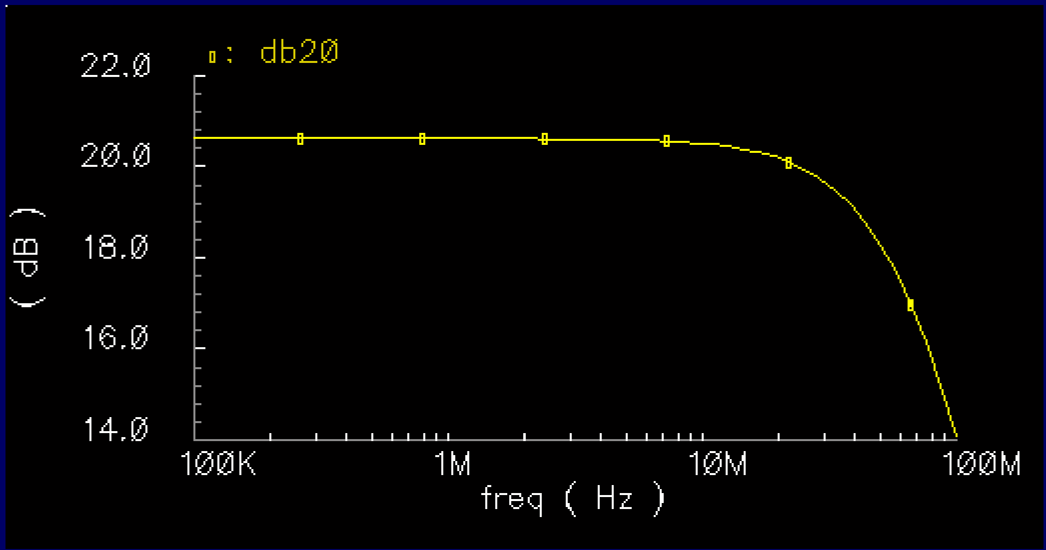
Compact amplifier layout



Chips design and layout aspects

Implementation of ASIC2

Compact amplifier AC simulation



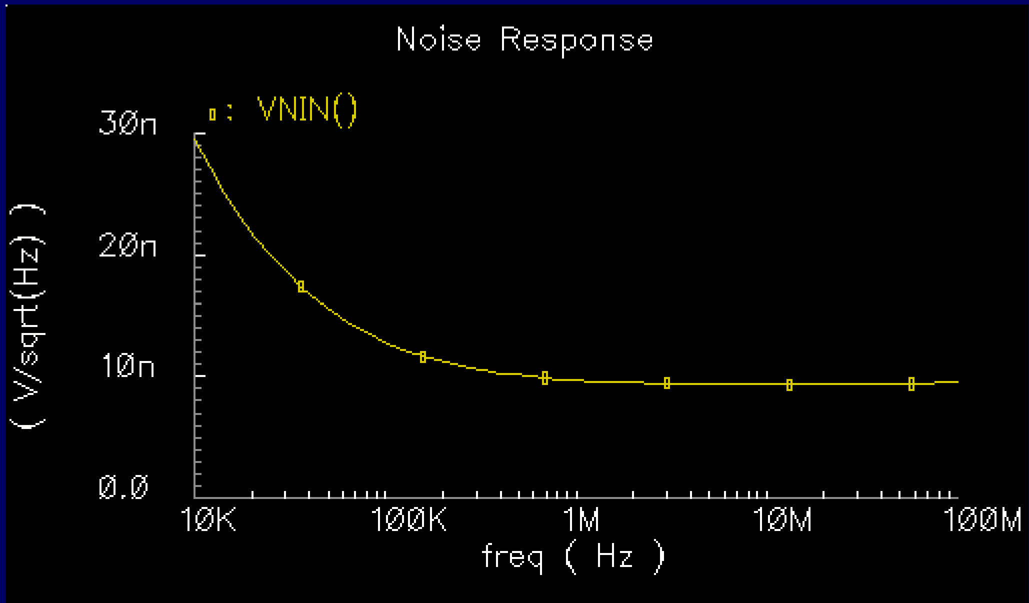
Load capacitance = 300 fF

-3 dB BW ≈ 60 MHz

Chips design and layout aspects

Implementation of ASIC2

Compact amplifier noise simulation

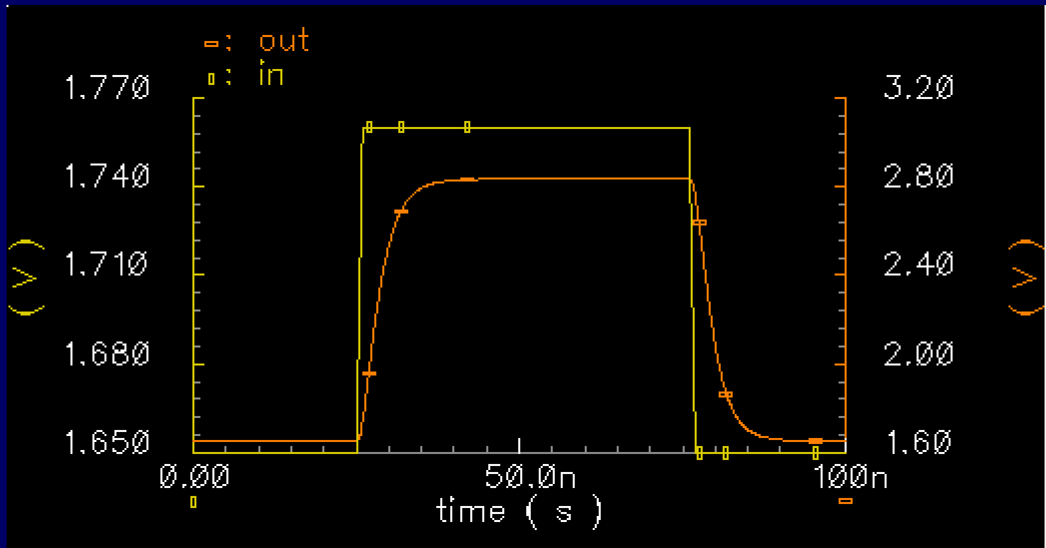


Input referred noise is commensurable with previous design

Chips design and layout aspects

Implementation of ASIC2

Compact amplifier stability simulation



Load capacitance = 300 fF

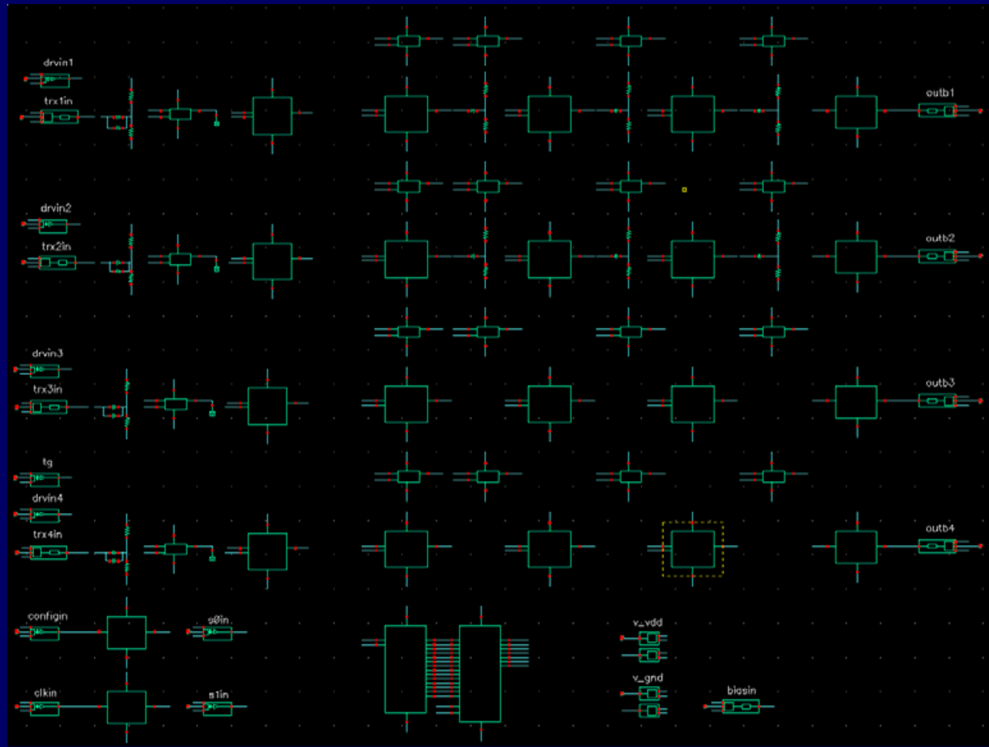
Chips design and layout aspects

Implementation of ASIC2

Four channel schematic

2 channels - with capacitive decoupling between amplifiers

2 channels- with DC inter amplifiers connections



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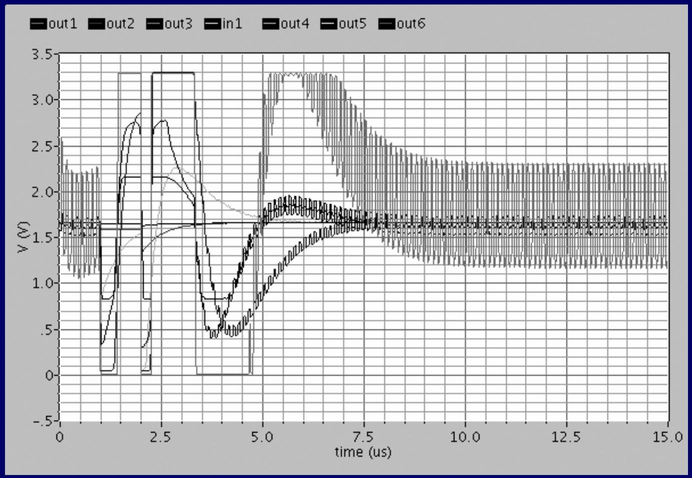
Chips design and layout aspects

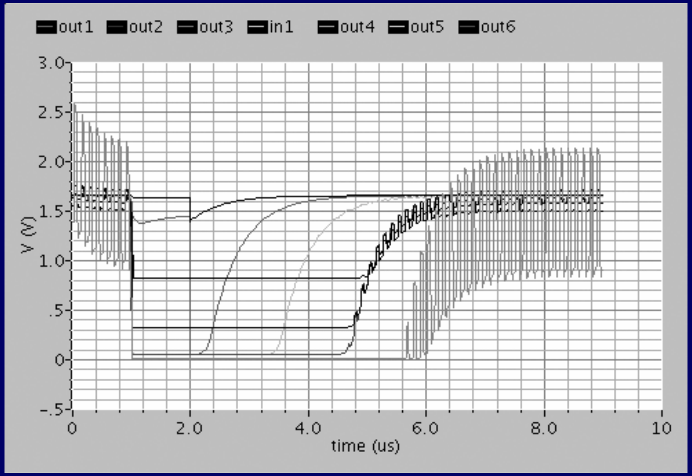
Implementation of ASIC2

Simulation of settling time

2 channels - with capacitive decoupling between amplifiers



2 channels- with DC inter amplifiers connections

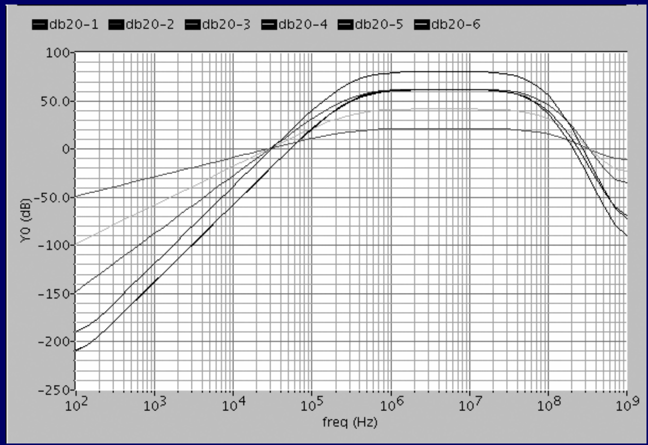


Chips design and layout aspects

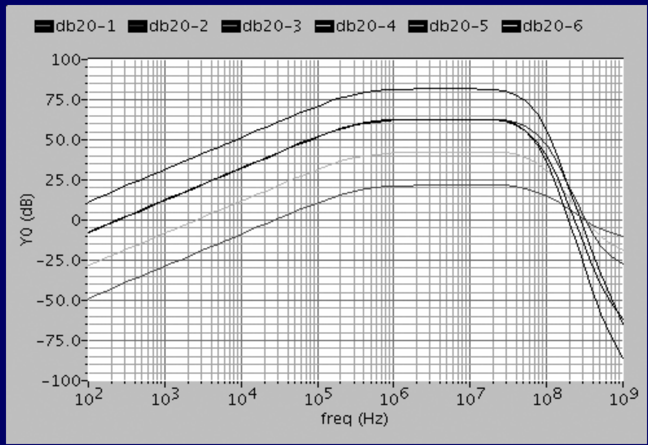
Implementation of ASIC2

AC simulation of amplifiers chain

2 channels - with capacitive decoupling between amplifiers

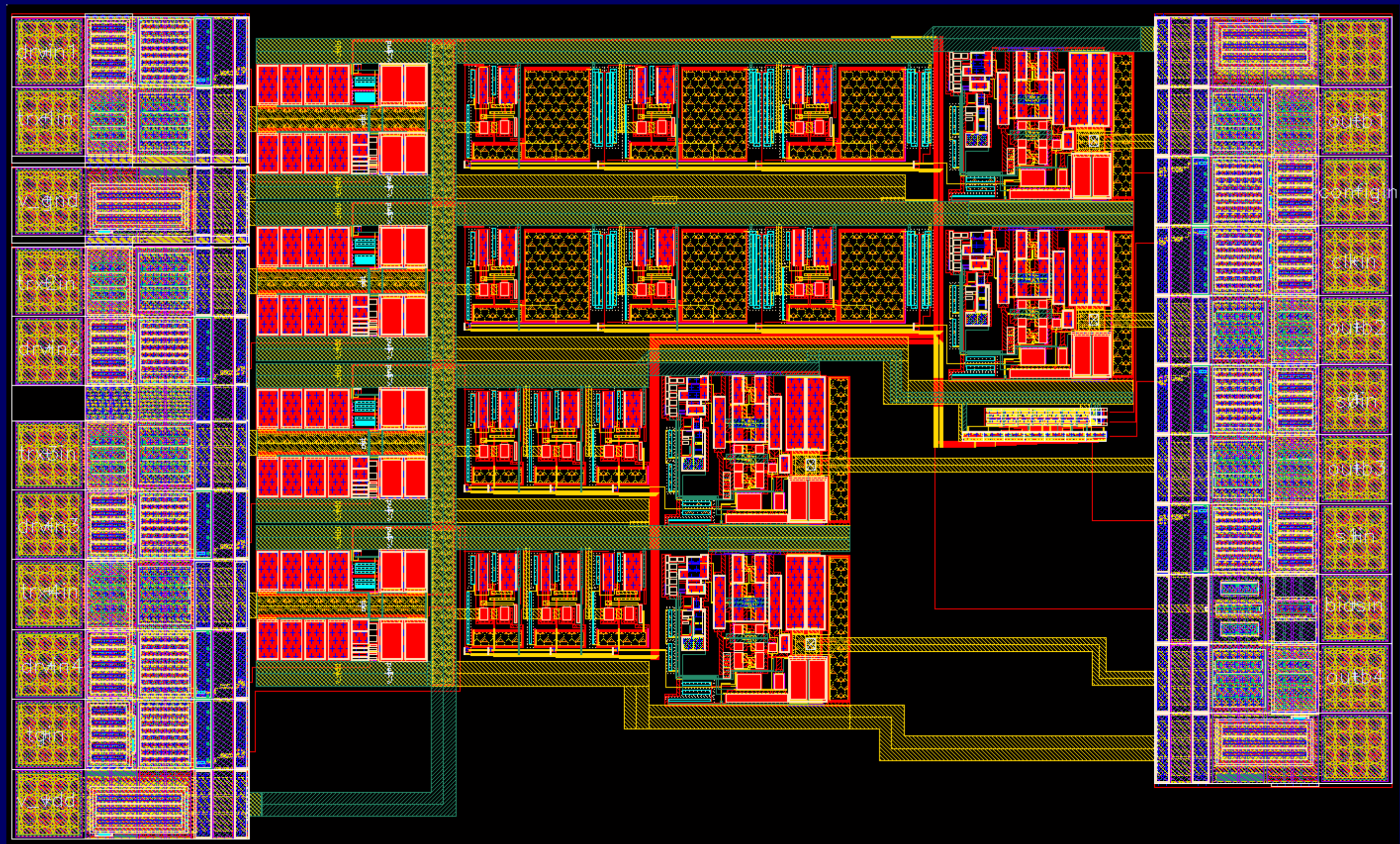


2 channels- with DC inter amplifiers connections



Chips design and layout aspects

Layout of of ASIC2



Chip test results

ASIC1

ASIC1 on test PCB

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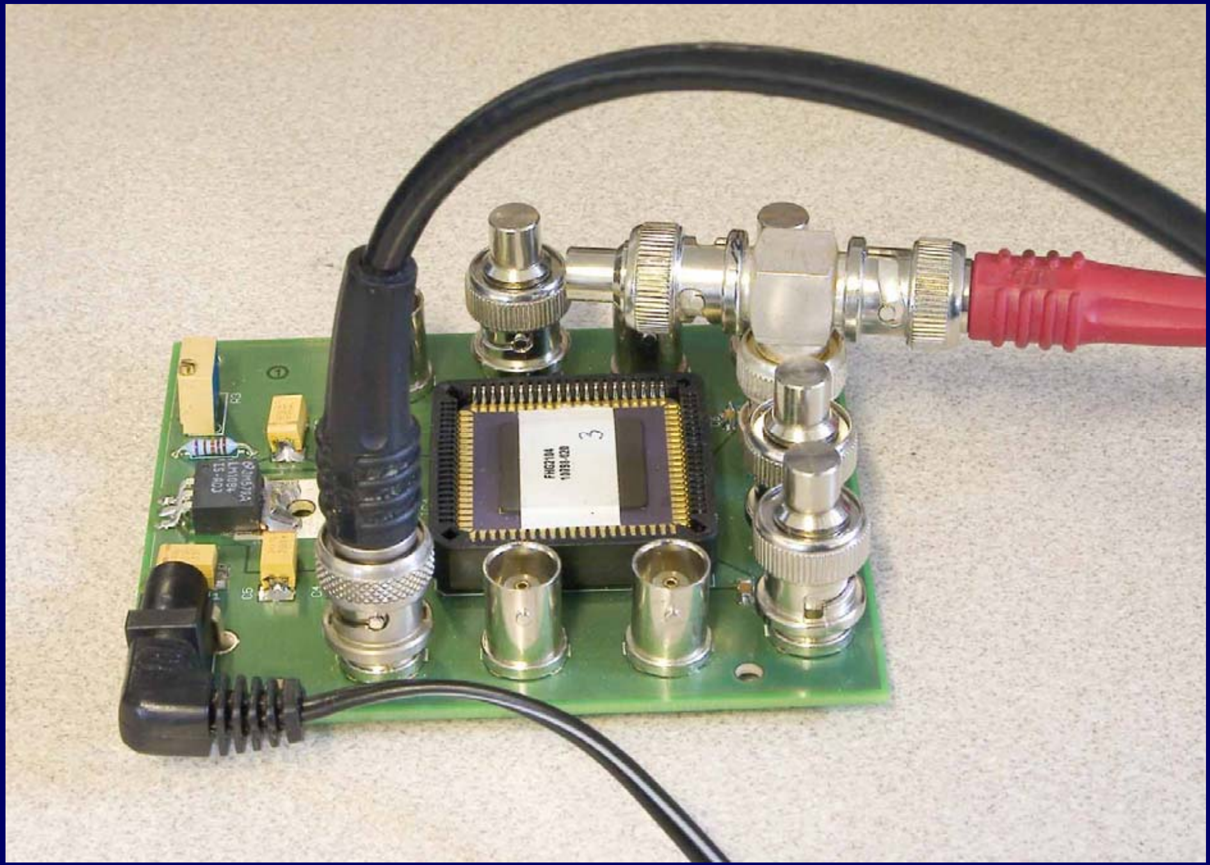
Chip test results

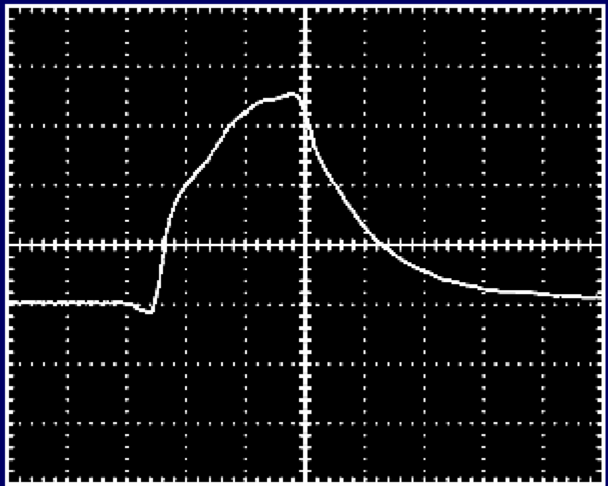
ASIC1



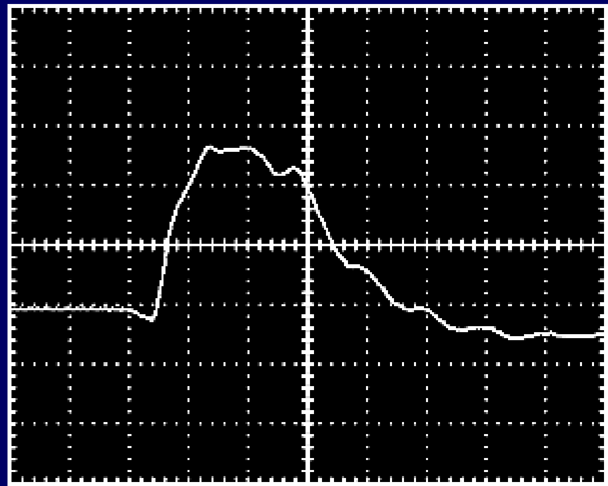
The board can be used as a pulser-receiver component

Chip test results

Results of driver's testing



a



b

Excitation driver response for 50 ns pulse

(a) – with 50 Ohm load

(b) – with Panametrics V317 20 MHz transducer load

Scale: ordinate axis – 0.5 V/div, abscissa axis – 20 ns/div

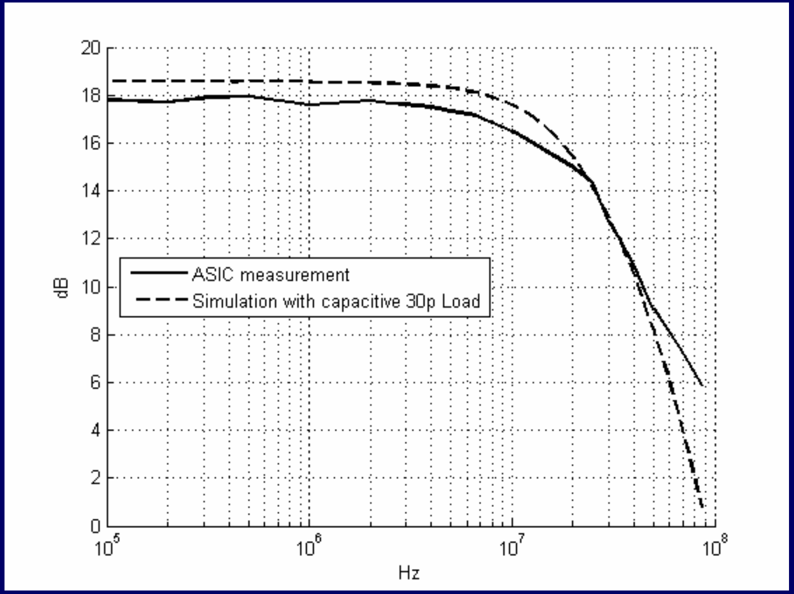
Chip test results

Results of driver's testing

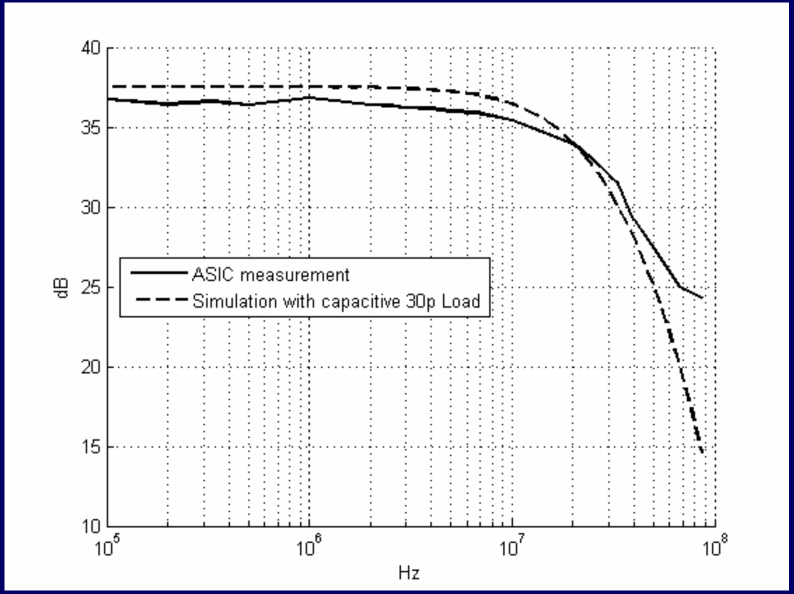
	Planned	Achieved
Supply voltage	3.3 V	3.3 V
Rise/fall time	20 ns	20 – 30 ns
High output impedance when inactive is provided by architecture		

Chip test results

Results of amplifier's bandwidth testing



a



b

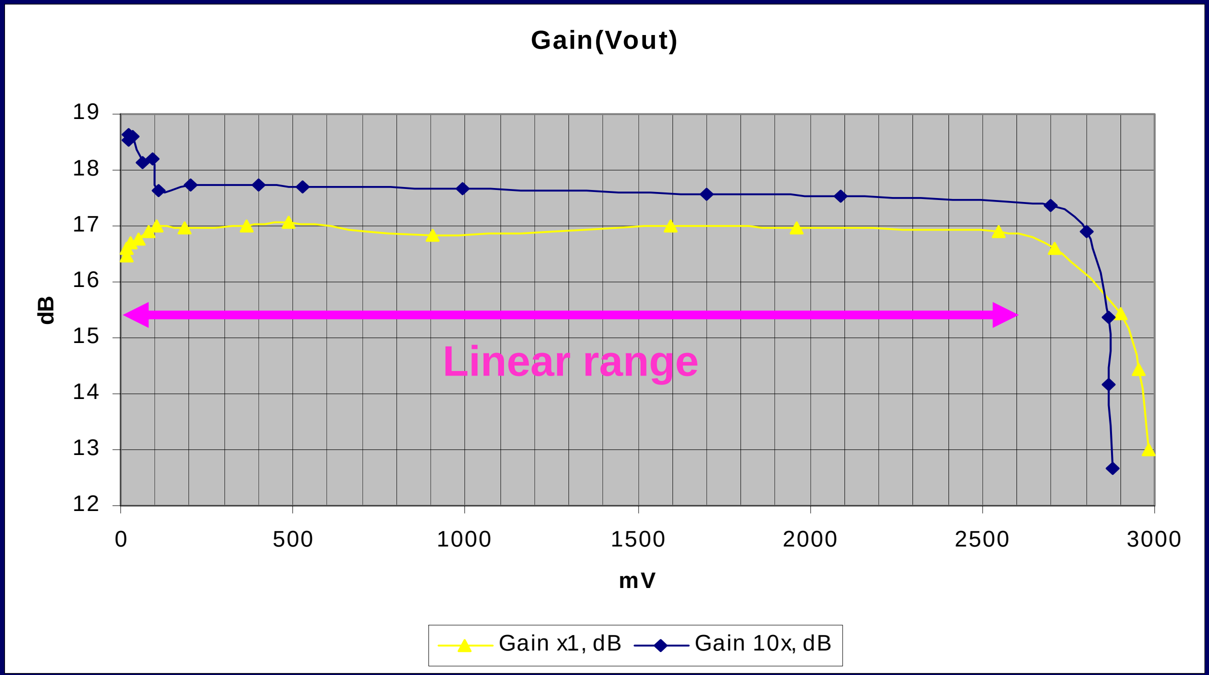
Comparison of experimental and simulated bandwidth for

(a) – single amplifier

(b) – cascaded amplifier

Chip test results

Results of amplifier's linear range testing

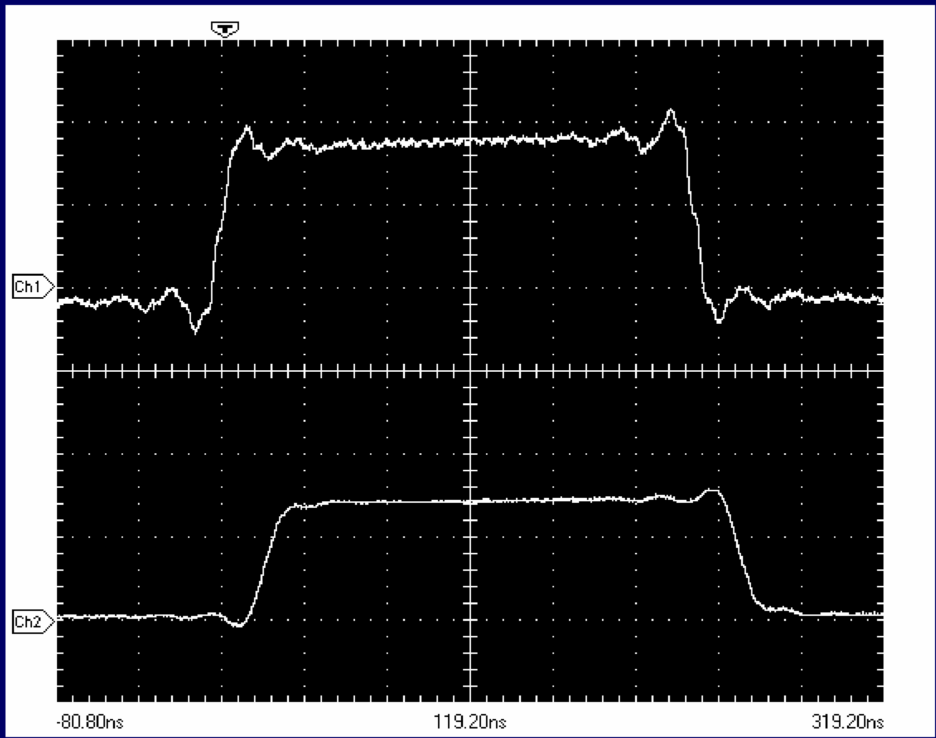


Gain according to output voltage

Gain x1 and Gain x10 are probe's settings

Chip test results

Results of amplifier's stability testing



Excitation by 0.1 V, 125 ns pulse

Scale: abscissa axis – 20 ns/div,

ordinate axis – channel 1 - 50 mV/div, channel 2 – 500 mV/div

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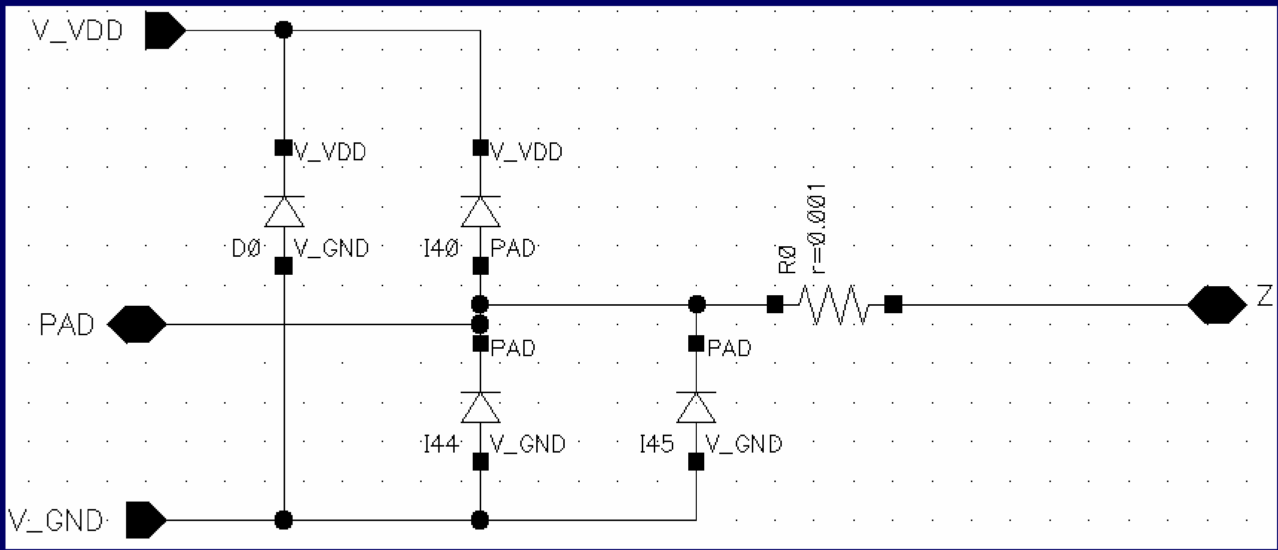
Chip test results

Results of amplifier testing

	Planned	Schematic	Hardware
Supply voltage	3.3 V	3.3 V	3.3 V
Bandwidth (5 pF load)	> 50 MHz	60 MHz	60 MHz
Bandwidth (30 pF load)		20 MHz	20 MHz
Gain (single amplifier)	~ 20 dB	18 dB	18 dB
Gain (cascaded amplifier)	~ 40 db	37 dB	37 dB
Input referred noise	23.7 $nV/Hz^{-1/2}$	10 – 20 $nV/Hz^{-1/2}$	18.74 $nV/Hz^{-1/2}$
Amplifier's output can bias similar amplifier			

Chip test results

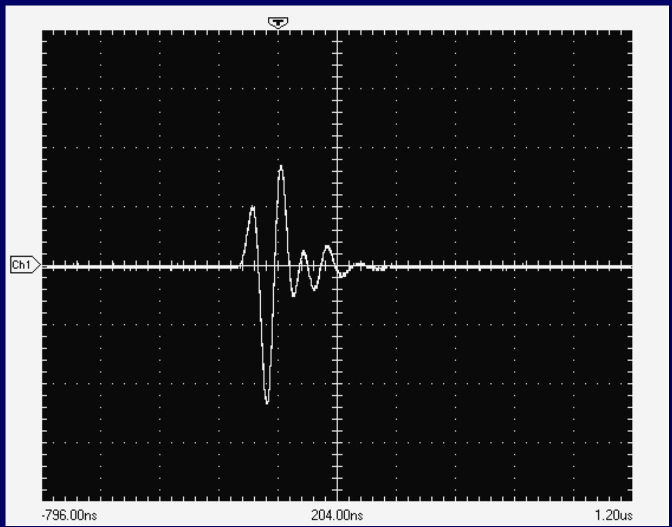
Utilization of pads' ESD protection for pulser-receiver mode

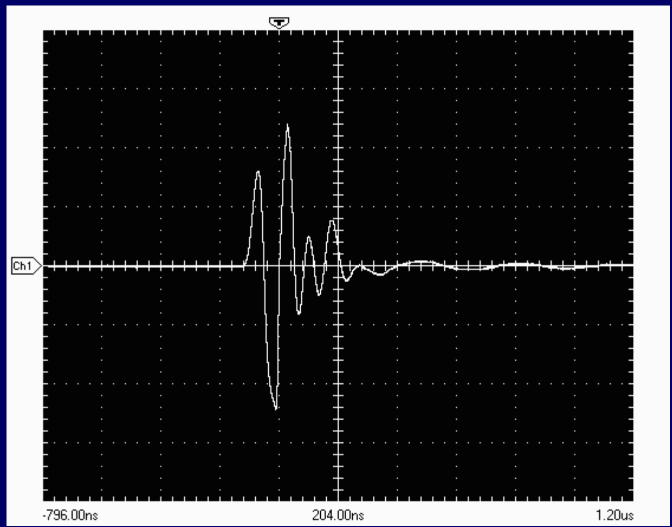


Schematic of utilized I/O pads with ESD protection

Chip test results

Testing of pulser-receiver component in through pulse mode





Pulse response acquired in through pulse mode with single amplifier,

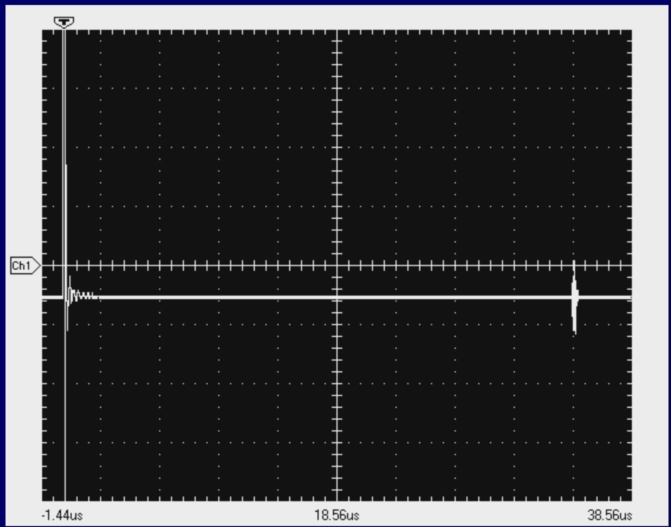
Scale: ordinate axis - 100mV/div, abscissa axis - 200ns/div

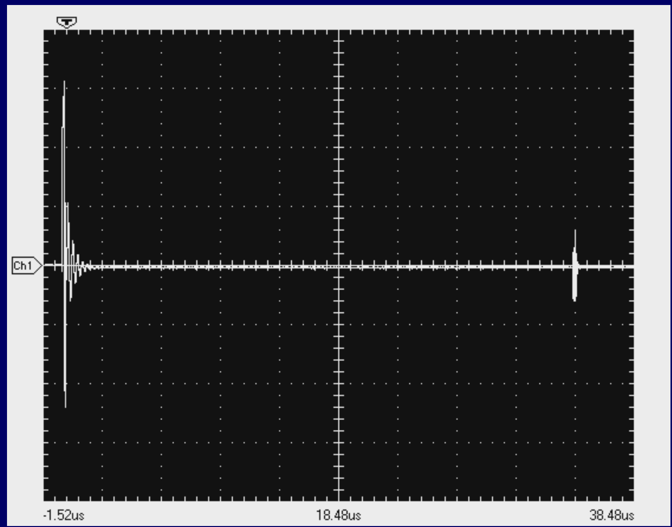
Pulse response acquired in through pulse mode with cascaded amplifier,

Scale: ordinate axis - 500mV/div, abscissa axis - 200ns/div

Chip test results

Testing of pulser-receiver component in pulse-echo mode





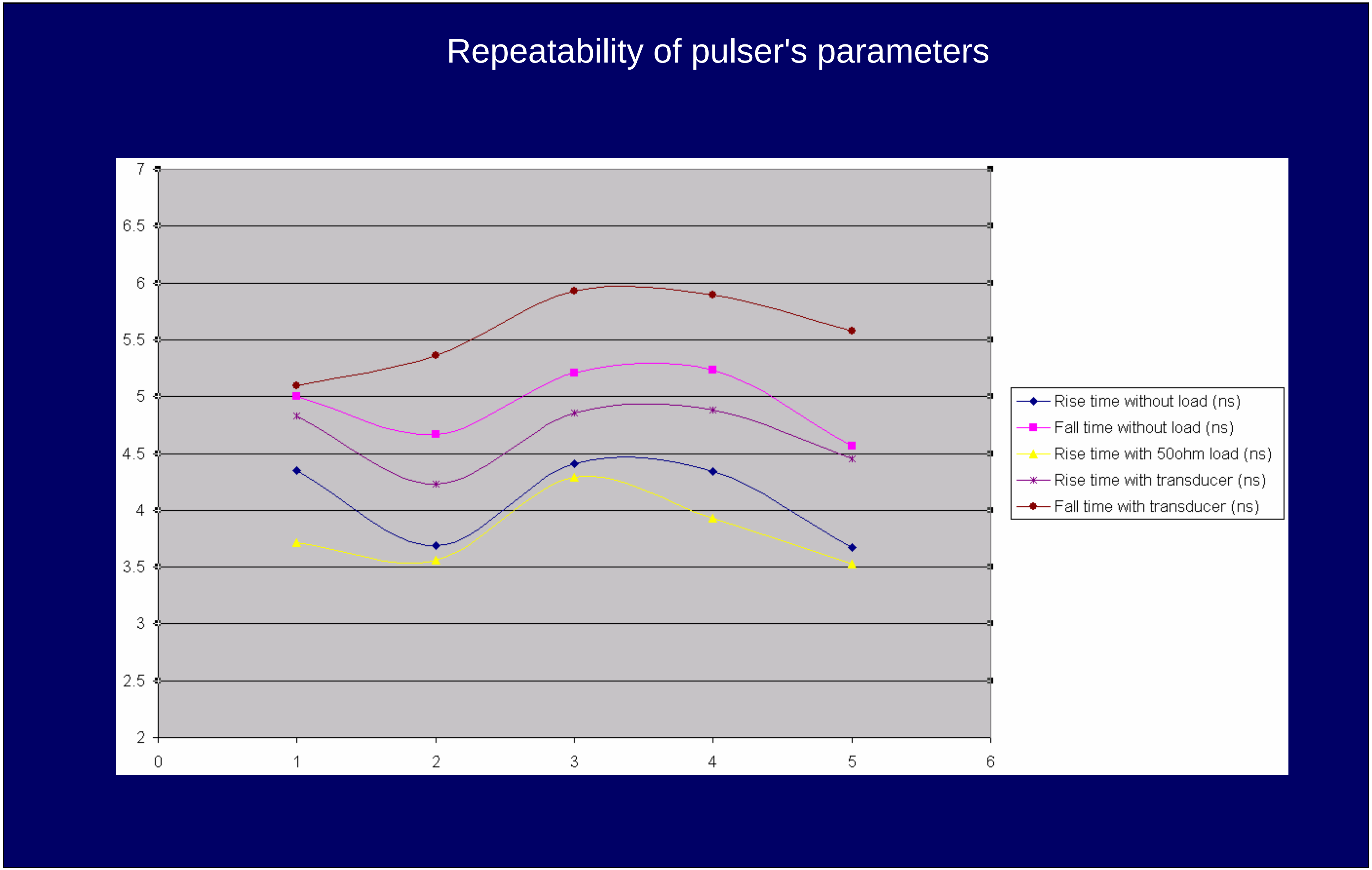
Recorded waveform for a single amplifier,

Scale: ordinate axis - 100mV/div, abscissa axis - 4μs/div

Recorded waveform for cascaded amplifier,

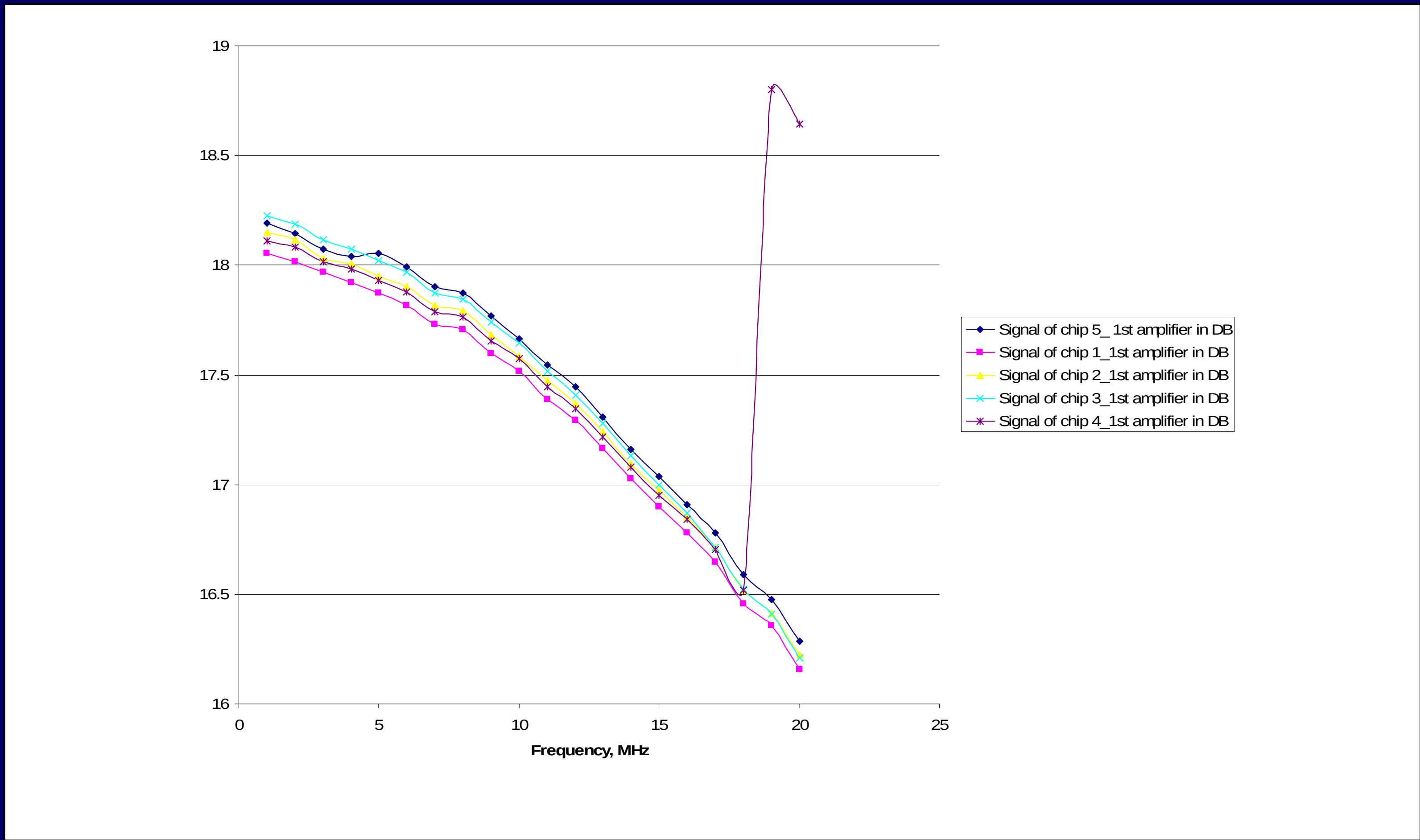
Scale: ordinate axis - 500mV/div, abscissa axis - 4μs/div

Chip test results



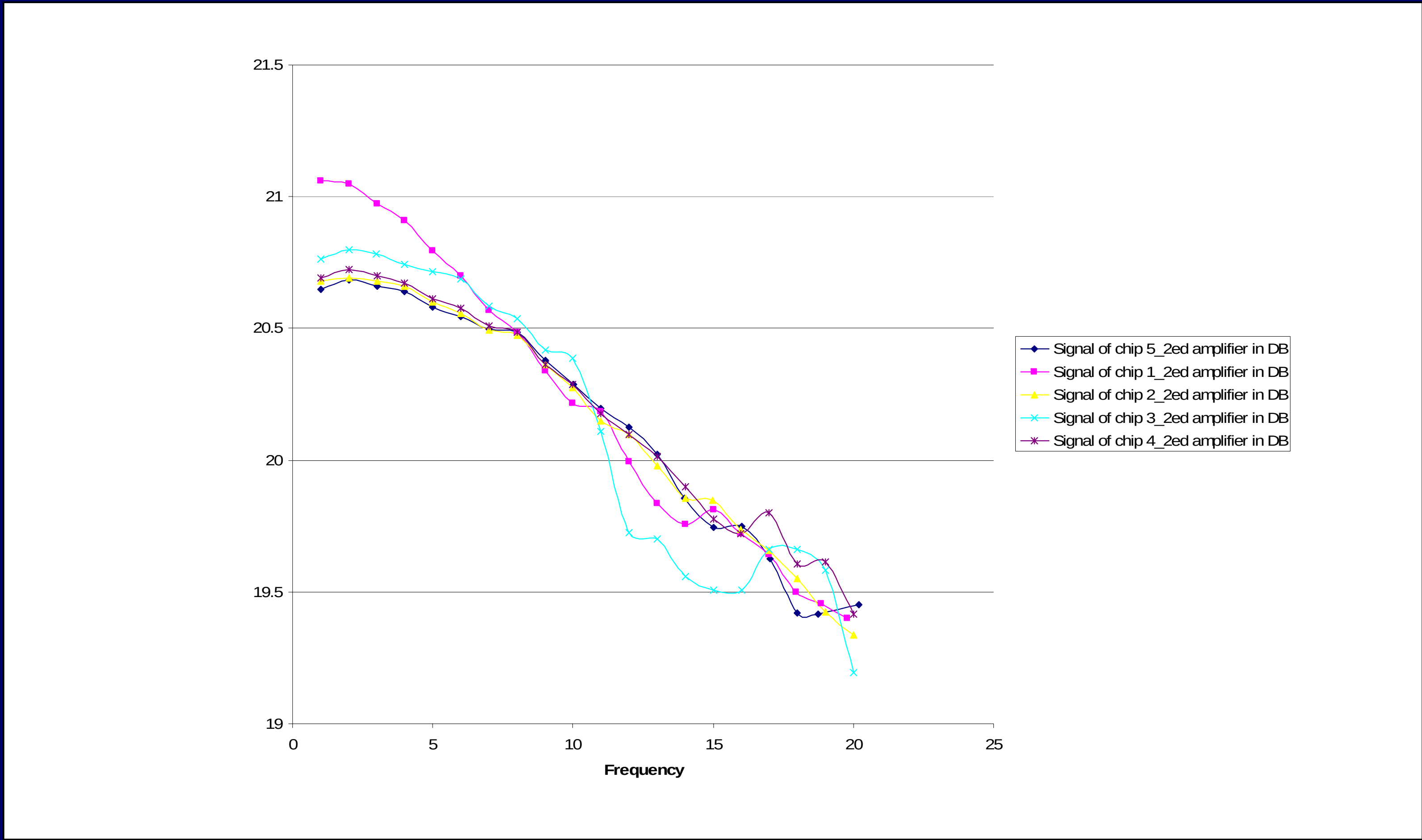
Chip test results

Comparison of amplifiers 1 gain among the 5 chips



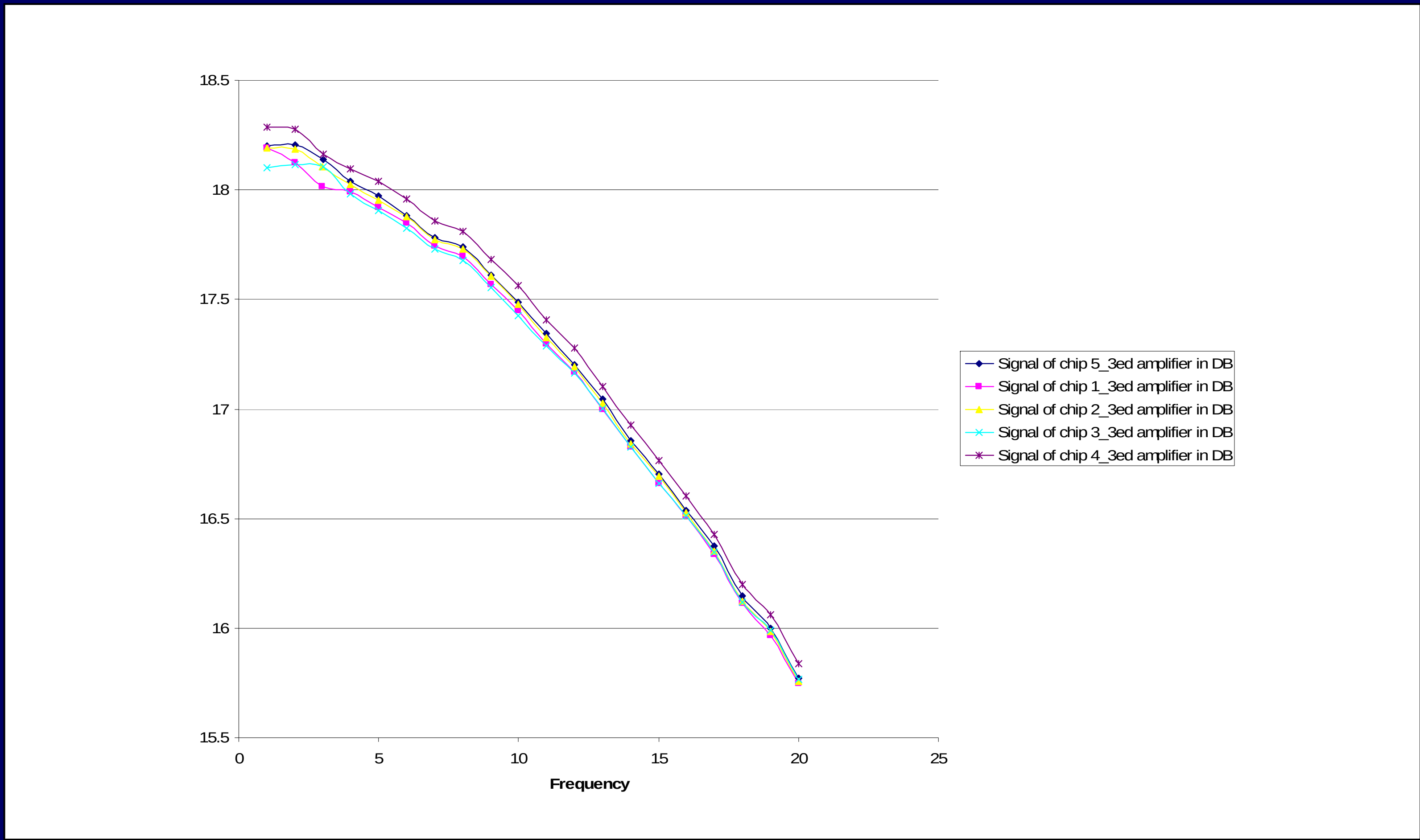
Chip test results

Comparison of amplifiers 2 gain among the 5 chips



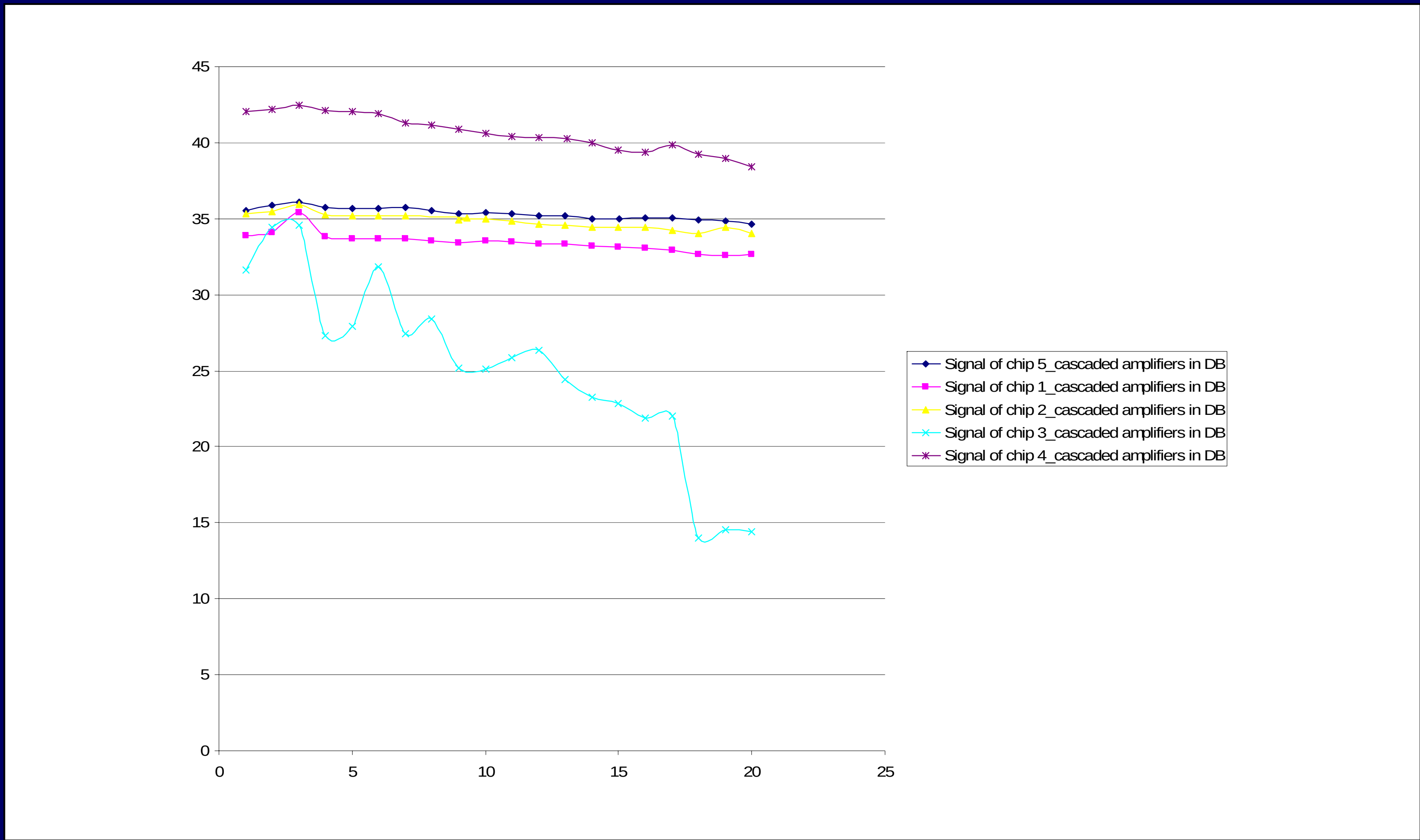
Chip test results

Comparison of amplifiers 3 gain among the 5 chips



Chip test results

Comparison of cascaded amplifiers gain among the 5 chips



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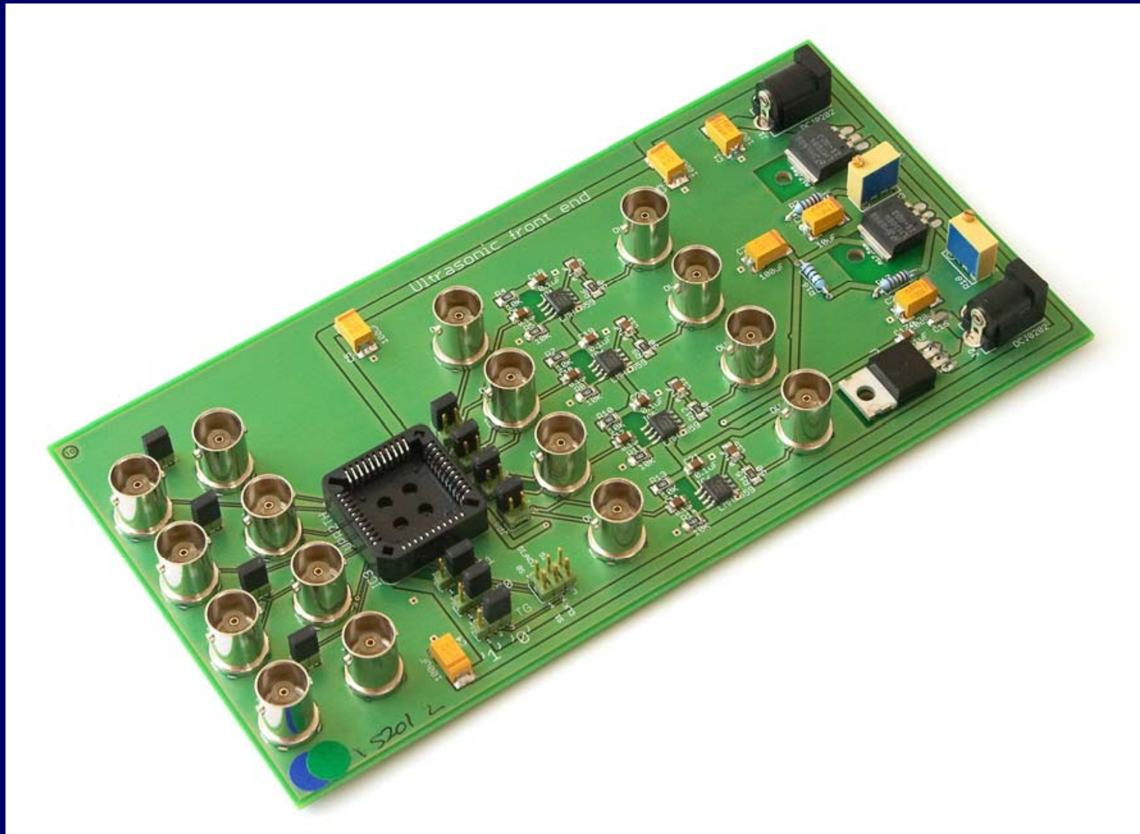
Chip test results

ASIC2



Testing board for ASIC2