High-Accuracy Data Acquisition Architectures for Ultrasonic Imaging

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***Abstract*—This paper proposes a novel architecture for a data acquisition system intended to support the next generation of ultrasonic imaging instruments operating at or above 100 MHz. Existing systems have relatively poor signal-to-noise ratios and are limited in terms of their maximum data sampling rate, both of which are improved by a combination of embedded averaging and embedded interleaved sampling. "On-the-fly" pipelined operation minimizes control overheads for signal averaging. A two-clock sampling timing system provides for effective sampling rates that are a factor of 20 or more above the basic sampling rate of the analog-to-digital converter (ADC). The system uses commercial field-programmable gate array devices operated at clock frequencies commensurable with the ADC clock. Implementation is via the Xilinx Xtreme digital signal processing development kit, available at low cost. Sample rates of up to 2160 MHz have been achieved in combination with up to 16384 coherent averages using the above-mentioned off-the-shelf hardware.**

I. Introduction

Ultrasonic inspection techniques are well established for remote nondestructive testing and evaluation, especially of opaque and/or conductive objects in medical diagnostics, science, and industry [1], [2]. Traditional ultrasonic measurements involve detection and/or estimation of the amplitude and delay of the excited pulse in the test medium that, when combined with a mechanical scanning technique, can be used to obtain images [3].

Imaging frequently involves beamforming when several appropriately delayed signals from different receivers are added together. This improves the signal-to-noise ratio (SNR) in a way similar to coherent averaging. Imperfections in time alignment in the time domain can degrade the performance of the beamformer in the same manner as frame jitter degrades the performance of an averager [4]. These imperfections decrease as the sampling frequency increases. Reconstruction of the desired image from raw records frequently involves a solution of some inverse problem [5]. However, the associated numerical procedures are highly sensitive to noise [6].

Recent developments have frequently linked parameters extracted from a raw ultrasonic record to a mathematical model of the observed phenomenon. Examples include: the assessment of bonding [7]; thickness measurement of oil films [8]; ultrasonic spectrography [9]; and the monitoring of chemical reactions at high resolution [10]. Small deviations of the recorded signal from a notional "true" signal caused by both electronic noise and imperfections of the data recorder often, however, results in significant uncertainty of the measurement outcome [11]. As a result, the accuracy of the data acquisition to a large extent determines the accuracy and resolution of images extracted from the raw records available.

The imperfections of the instrument are predominantly associated with its analogue part and the analog-to-digital converter (ADC). The latter is characterized by its temporal (sampling frequency) and amplitude (number of output bits) resolutions. Flash ADC architecture ensures the fastest conversion at a cost of increased hardware complexity that limits the achievable amplitude resolution [12]. This amplitude resolution can be improved by using several flash ADCs in a pipelined chip (i.e., subranging converters [12]), and this solution is implemented widely in many commercially available ADCs. To ensure that the quantization noise remains negligible, it should be smaller than the input additive noise (the internal noise of the receiver amplifier plus the noise caused by electromagnetic interference). Twelve bits or more can be considered as sufficient for an accurate recording of waveforms with an SNR of 60 dB or less, which is typical for ultrasonic measurements.

Temporal resolution can be enhanced by interleaving samples converted by several ADCs either on chip [13] or on board [14]; however, these implementations require accurate clocking and careful consideration of mismatch effects [15], [16]. To avoid these complications, and in order to decrease the component costs and development time, most ultrasonic instruments are built around a single ADC. Software interpolation of relatively sparse samples, although used in some ultrasonic instruments [17], relies heavily on the quality of the raw records and thus to some extent is inherently limited. At the time of writing (Spring 2006), the top-of-the-range ADCs have sampling frequencies above 1 GHz, costing typically 1 kUSD for an 8–10 bits resolution, whereas the cost of commercially available data acquisition boards that utilize these ADCs can easily reach 10 kUSD. Currently, ADCs with sampling frequencies of around 100 MHz are more widely available and are, of course, considerably less expensive. These are insufficient for the more advanced ultrasonic requirements. For example, broadband ultrasonic pulses are normally sampled at 10 (and more) times the central frequency [8], [9].

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This central frequency could be: from 50 MHz for conventional focused transducers [3]; to 100 MHz and above for polyvinylidene fluoride and capacitive micromachined ultrasonic transducers (cMUTs); 200 MHz or higher for laser ultrasound [18], [19]; and ultimately around 1 GHz for acoustic microscopes [20]. These high frequencies are essential to achieve a high spatial resolution on the order of microns for thin film thickness measurements [8] and the examination of biological cells [20], for example.

The other potential major source of measurement error is the electronic noise of the receiver amplifier that often far exceeds the quantization noise of modern ADCs. This is due to an exponential increase of the ultrasonic attenuation with frequency that severely worsens the SNR for the same level of noise. (For example, in one of our recent experiments, a sonification of a sapphire window of a biological reactor showed that, despite the excitation voltage being set to 100 V, a 20-MHz pulse propagated for 7 μs in a pulse-echo mode required an amplification of 46 dB in order to fully utilize the ± 1 V range of the deployed ADC. Here we found that the RMS of the additive noise, even after 64 averages, was approximately 1 mV, which far exceeded the 0.125 mV quantization step of the 14-bit ADC utilized.) Noise reduction is frequently achieved by using either analogue (e.g., the "boxcar" technique [21]) or the preferable digital averaging methods [1, p. 154]. Often the disadvantage of digital averaging instruments is their considerable time required for averaging. We have found that commercial equipment purchased for our laboratory has processing times of over 10 seconds for 1,000 averages, even when the ultrasonic pulse repetition frequency is over 1 kHz, where one would expect the averaging to be completed potentially within 1 second.

As a result, we have identified a requirement for a new improved high-accuracy data acquisition architecture for custom ultrasonic applications that combines fast averaging with significantly higher sampling rates than is possible with conventional approaches. This proposed new architecture is the subject of this paper.

The paper is organized as follows. Section II states the design objectives, and outlines the development environment and tools. Section III presents the averaging architecture that processes incoming samples as they become available from the ADC, making the averaged waveform available as soon as the required number of excitations has taken place. Section IV describes a frame interleaving architecture that ensures an increase of the equivalent sampling frequency of the ADC by an integer factor. The integration of the above-mentioned architectures is described in Section V. Section VI contains relevant details of the implementation, and examples of experimental waveforms. The paper is concluded by Section VII.

II. Design Objectives

Two important aspects of commercial digitizing systems as they have developed over the years is their continuing reduction in cost—around three orders of magnitude in a decade—and their rapid obsolescence, which can result in a high cost of ownership overall. We see advantages in the development of generic systems that can be realized in a continuously developing manner, using electronic components that themselves evolve in their functionality and with reducing cost. Reconfigurable hardware is relevant here and, in this respect, field-programmable gate array (FPGA) integrated circuits offer powerful development platforms. FPGAs can be reconfigured many times and so rapid prototyping is possible using the powerful software tools and hardware kits available commercially. In this work, we have selected the Xilinx Xtreme digital signal processing (DSP) development kit (Xilinx, San Jose, CA) as our development platform; it offers convenient design software, a multi-million gate FPGA, on-board ADCs and digital-to-analog converters, and a computer interface.

An important objective of our design was to achieve the clock frequency of a digital control part commensurable with the ADC clock frequency. In this case, the design can be applied to many commercially available DSP boards that include an ADC and a processing element capable of clocking at the same frequency.

Finally, we intended to use the highest level design tool possible. Xilinx System Generator version 6.3 satisfied most of the design needs, and ensured rapid alterations of the design needed in the research environment. A piece of a custom very (high speed integrated circuit) hardware descriptive language (VHDL) code was required to be developed, though, to allow independent control of the on-chip oscillators.

III. Zero Overhead Averaging Architecture

Software implementation of the digital averaging involves storing the ADC output data into a processor-accessible memory. The processor can be connected to the ADC directly or through a first in, first out buffer (programmed input). Alternatively, the direct memory access via a dedicated bridge can be employed. After the acquisition of the current data frame, the processor updates the running average. If memory requirements are to be minimized, ADC output data are placed into a BUFFER area of memory and the accumulating averaged record is placed in an identified location, AVER, say. The following pseudocode illustrates the operations involved:

```
AVER=0;
for (j=0;j<Naver;j++)
      { //acquire new frame into BUFFER;
        for (i=0;i<Nsamples;i++)
              AVER[i]+=BUFFER[i];
      }
AVER/=Naver;
```

It will be clear that every sample that is taken into the average requires three memory accesses, setting significant

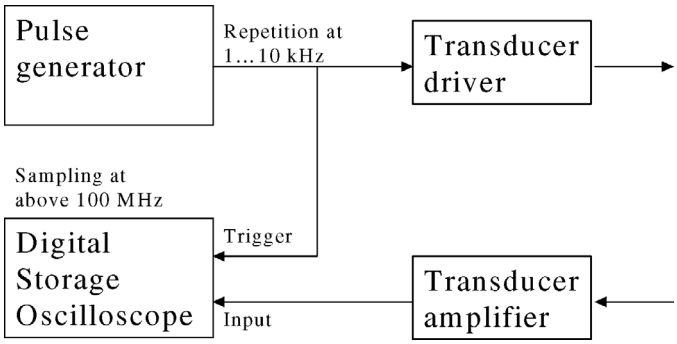

Fig. 1. Typical arrangement for ultrasonic measurements using stand-alone instruments.

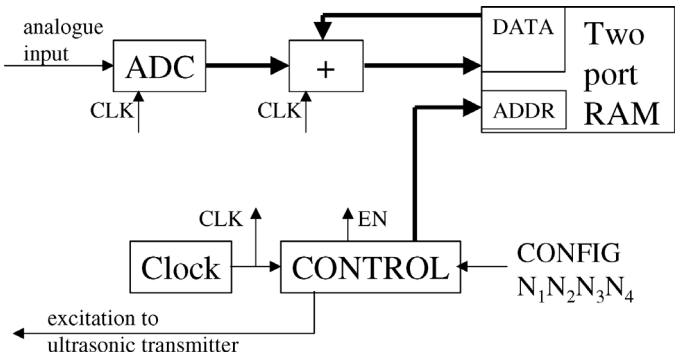

Fig. 2. Zero overhead averaging architecture.

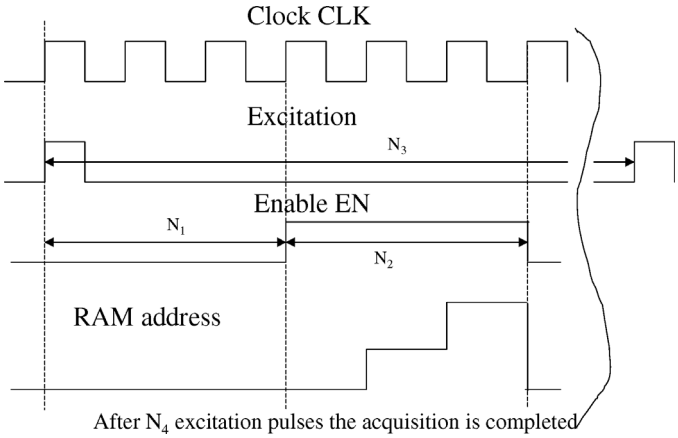

Fig. 3. Time diagrams for zero overhead averaging architecture.

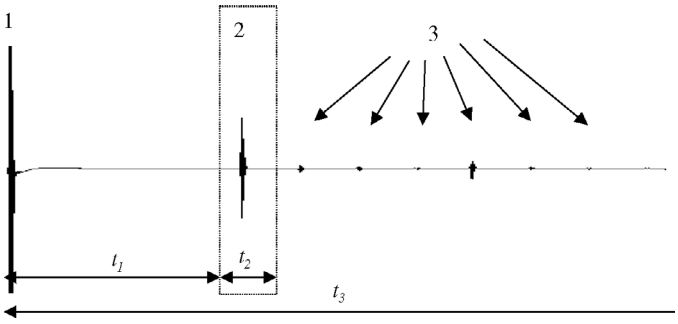

Fig. 4. A typical signal record in the time domain. (1) is the excitation signal breakthrough, (2) is the window of interest, and (3) consists of parasitic multiple reflections. The origin of time ($t = 0$) is the point of transmission, and t_1 is the time delay to the data acquisition trigger.

limitations on overall acquisition speed. Many commercially available data acquisition boards do not offer averaging, which then has to be implemented by the user at the host computer level, again significantly limiting overall acquisition speed. Digital storage oscilloscopes (DSOs) can provide high sampling rates with averaging as standard. Generally, their specifications exceed those of the best ADCs, by dint of careful proprietary design. They are expensive but in many instances may offer the only workable option for high-frequency ultrasonic systems [20]. A typical arrangement for an ultrasonic system that includes a DSO is shown on Fig. 1; it is suitable for one-shot measurements but may introduce uncertainties in the acquired data when the data are averaged as an ensemble of records. The reason for this is that separate oscillators clock the ultrasonic transmitter and the digitizing operation within the DSO, and this leads to random time delays between the ultrasonic system trigger and the start of the acquisition of each frame of data. These delays result in some temporal incoherence between successive records in a coherent average [4]. Any system designed to overcome this problem must provide tight synchronization between the ultrasonic system clock and the frame trigger associated with the digitizer proper.

The architecture shown on Fig. 2 illustrates how we have addressed the issues discussed above. It provides averaging of successive records as they are acquired, as well as close synchronization between the ultrasonic transmitter (excitation) and the data acquisition system. In principle, and depending on the hardware used, it can be upgradable without undue effort or cost. An adder [+] between the ADC and memory provides for coherent averaging at the maximum possible speed; the use of a dual-port RAM enables the adder to be supplied with the accumulating average at the same time as data are acquired from the ADC, minimizing demand for memory overall. The control unit uses the four timing inputs shown on Fig. 3. N_1 and N_2 determine the data acquisition window width as a number of clock cycles, N_3 sets the frame repetition rate, and N_4 sets the number of averages. In practice, these parameters are down-loaded from the host computer at initialization. When the averaging cycle completes, the system communicates with its host via a dedicated interface. Considering now how this system would be integrated into an ultrasound propagation experiment, we refer to the typical ultrasonic record shown on Fig. 4. Assume that we wish to estimate the time delay t_1 before the signal of interest that is the first reflected echo set in the window t_2. The delay t_1 is related to the propagation path l and the wave speed c by the conventional time of flight equation,

$$t_1 = 2\frac{l}{c}. \tag{1}$$

The duration of the acquisition window t_2 is determined by the center frequency of the transducer and its bandwidth;

it is generally sufficient to capture between five and ten cycles of the response, giving

$$t_2 > \frac{5..10}{f_0}. \tag{2}$$

The time interval between successive frames of data t_3 has to be great enough for multiple acoustic reverberations to die away, and this depends on the absorbing and scattering properties of the test medium, the propagation distance and wave speed, and the acoustic impedance mismatches at either end of the wave path. Typically t_3 will be around 1 ms. The timing parameters are determined thus:

$$\begin{aligned} N_1 &= \text{int}\,[t_1/t_s]\,, \\ N_2 &= \text{int}\,[t_2/t_s] + 1, \\ N_3 &= \text{int}\,[t_3/t_s] + 1, \end{aligned} \tag{3}$$

where t_s is the reciprocal of the sampling frequency f_s. An additional condition that applies to N_2 is that it should not exceed the available depth of RAM. The choice of the number of averages, N_4, involves a trade-off between the required increase in SNR, ΔSNR, say, and the total available measurement time t_m.

$$\begin{aligned} t_m &= N_4 * t_3, \\ \Delta\text{SNR,dB} &= 10 \log_{10}\, N_4. \end{aligned} \tag{4}$$

Generally, the number of averages required increases with transducer operating frequency, simply because the attenuation in most materials is a rising function of frequency. It was observed that in most experiments around 1024 averages represent a workable compromise.

Further details of implementation of the averager alone, results of its experimental operation, and assessment of its performance were reported elsewhere [22]. The effect of averaging can be seen from figures presented in Section VI by comparing graphs (b) with graphs (d) that show a substantial reduction of the additive noise by a factor of $\sqrt{512/2} = 16$.

IV. Two Clock Accurate Frame Interleaved Sampling Architecture

The achievable sampling rate of an integrated ADC is limited by its manufacturing technology. Using several ADCs in a time interleaved mode [13], [14] allows us to exceed this limit. However, this results in a rapid increase in a cost of the ADC parts and their interconnect. Techniques developed for recording very rare short pulses do not seem to be applicable directly for ultrasonic instruments either (for example, because of use of special application-specific integrated circuits [23] or potentially ill-conditioned signal restoration procedures [24]).

Random interleaved sampling (RIS) is a general-purpose approach to high-speed digitization that relies on the availability of an ensemble of identical signal records. It uses a single ADC that samples all of the records many times at its maximum clock frequency. The records acquired are interleaved in memory according to their (random) frame shift related to an external trigger event. The equivalent sampling frequency depends on the accuracy of the quantification of the delay, and could be as high as 100 GHz for a digital storage oscilloscope or from several GHz up to 50 GHz for a high-performance data acquisition board. This technique works if and only if the subsequent records are identical [25]. A drawback of this approach is that, even with a high number of records acquired, there is no guarantee that all possible delays would occur, and this results in a requirement for post-processing and a demand for many more records than the simple ratio of the equivalent sampling frequency to the ADC sampling frequency would suggest.

Another approach that utilizes the availability of an ensemble of "identical" records was developed for equivalent time and on-chip oscilloscopes [26], and involves control of the excitation. One oscillator triggers the excitation whereas another oscillator operating at lower frequency triggers the acquisition. Due to the frequency difference, the acquisition instant is delayed differently for every subsequent excitation pulse. This approach intends to acquire a single sample per a single excitation, and is not therefore suitable either for acquisition of long records or for averaging. For example, acquiring 1,000 samples for a single record would require 1 s at the pulse repetition frequency of 1 kHz, even without averaging.

This principle is applicable for ultrasonic imaging if the test medium is not evolving too fast. In our experiments, the media could be considered stationary for several seconds at least. Therefore repeating the excitation pulse at several kHz allows collecting enough coherent records for both averaging and interleaved sampling.

The advantages of RIS (acquisition of more than one sample per frame) and using two different clocks for excitation and acquisition (accurate timing) were combined in this development, and targeted a commercially available FPGA chip. Multiple clock sequences required for sampling an ensemble of records were achieved by using two oscillators whose frequencies precisely satisfied the following relationship:

$$mf_1 = (m+1)f_2, \tag{5}$$

where $m \in N$. This condition implies that, if the rising edges of the oscillators coincided at some instant t_0, they would exactly coincide again at

$$t_k = t_0 + k\frac{m}{f_2} = t_0 + k\frac{m-1}{f_1}, \quad \forall k \in N. \tag{6}$$

The timing diagram for the case $m = 3$ is presented in Fig. 5. The very close synchronization that is required in this system can be achieved, for example, by using digital clock managers (DCMs) available on Xilinx FPGA chips. These DCMs are capable of generating several related and tightly synchronized clock sequences. The synchronized oscillators are used for clocking two otherwise completely

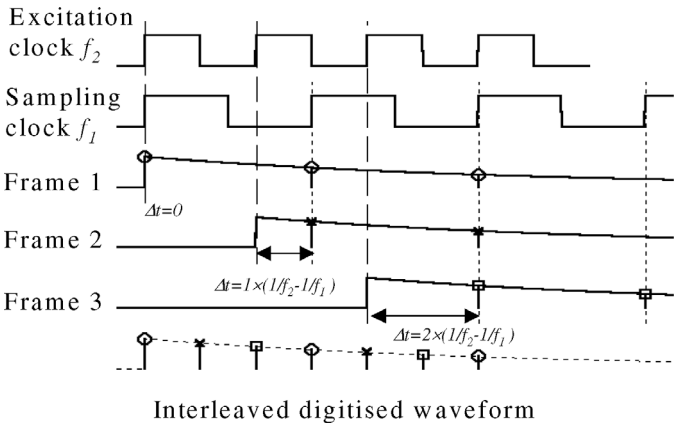

Fig. 5. Time relations between two-clock sequences for a frequency ratio 3:2 providing three different delays.

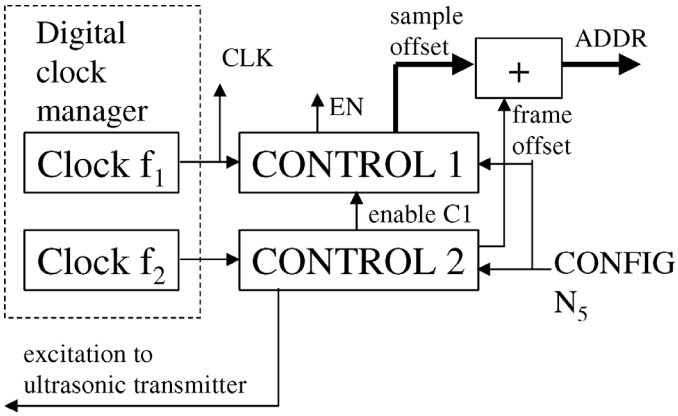

Fig. 6. Two-clock frame interleaved sampling architecture.

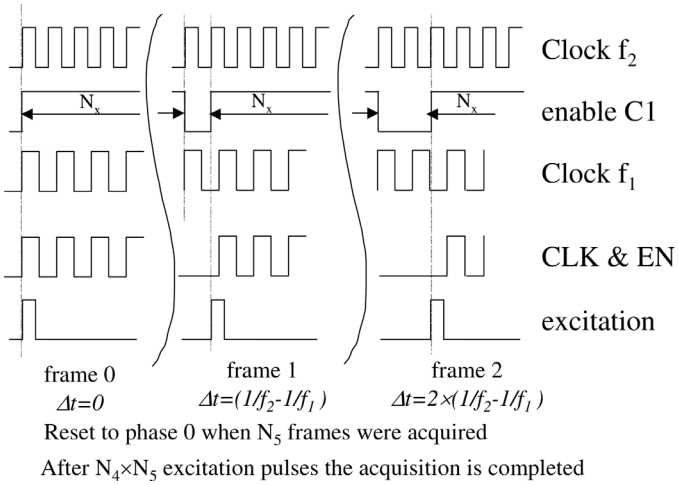

Fig. 7. Time diagrams for two-clock frame interleaved sampling architecture with averaging.

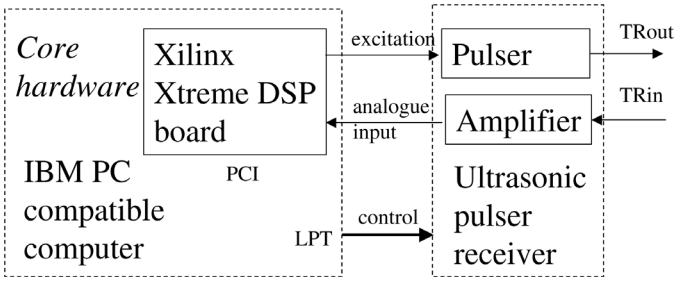

Fig. 8. Block diagram for a complete experimental setup.

separate circuits—the excitation trigger (higher frequency, f_2 in Fig. 5) and the ADC (lower frequency, f_1 in Fig. 5). At the first repetition of the excitation, the edges of the clocks coincide with each other (frame 1, Fig. 5). The first pulse of f_2 shown in Fig. 5 triggers the excitation. The ADC samples an input signal with zero delay relative to the edge of the excitation pulse (samples showed with circles for an exponentially decayed input wave, Fig. 5). At the second repetition, the excitation trigger is associated with the second pulse of f_2. The ADC starts sampling after the excitation trigger from the second pulse of f_1. This ensures a delay between the excitation and the sampling sequence of $1/f_2 - 1/f_1$ (frame 2, samples are indicated in Fig. 5 by crosses). At the third repetition, the third pulse of f_2 triggers the excitation pulse. The ADC is clocked with the delay of $2 \times (1/f_2 - 1/f_1)$ to the excitation trigger, that is, frame 3 (Fig. 5, squares on the top of the samples). The acquired samples are interleaved in RAM (Fig. 5 at the bottom), and the RAM address is incremented by m (rather than 1) for every successive sample in the same frame; the addresses in every successive frame are offset from the previous frame by 1.

An extended description of this architecture, its comparison with other alternatives, and discussion of its advantages related to power consumption can be found elsewhere [27]. The effect of the interleaving can be seen from figures presented in Section VI by comparing graphs on the left with the graphs on the right.

V. A Combined Interleaving and Averaging Architecture

An analysis of the interleaving and averaging architectures described above shows a possibility of their integration into a single design. After the acquisition of the last frame (third frame for $m = 3$, Fig. 5) the RAM address offset is reset to 0, thus enabling the coherent acquisition of a new completed waveform for averaging. The block and associated timing diagrams related to this architecture are presented in Fig. 6 and Fig. 7, respectively. The configuration parameters now include one extra parameter N_5 that specifies the number of frames and is tied to the relation between the clock frequencies used ($N_5 = m$). After counting N_3 pulses of the clock f_2, the CONTROL 2 block skips a number of pulses equal to the frame number and produces the excitation and enable C1 signals. The number of the current phase is used as an offset for the RAM address as well. The restriction on the allowable value of N_3 required for ensuring coincidence between the clocks is that the following should hold:

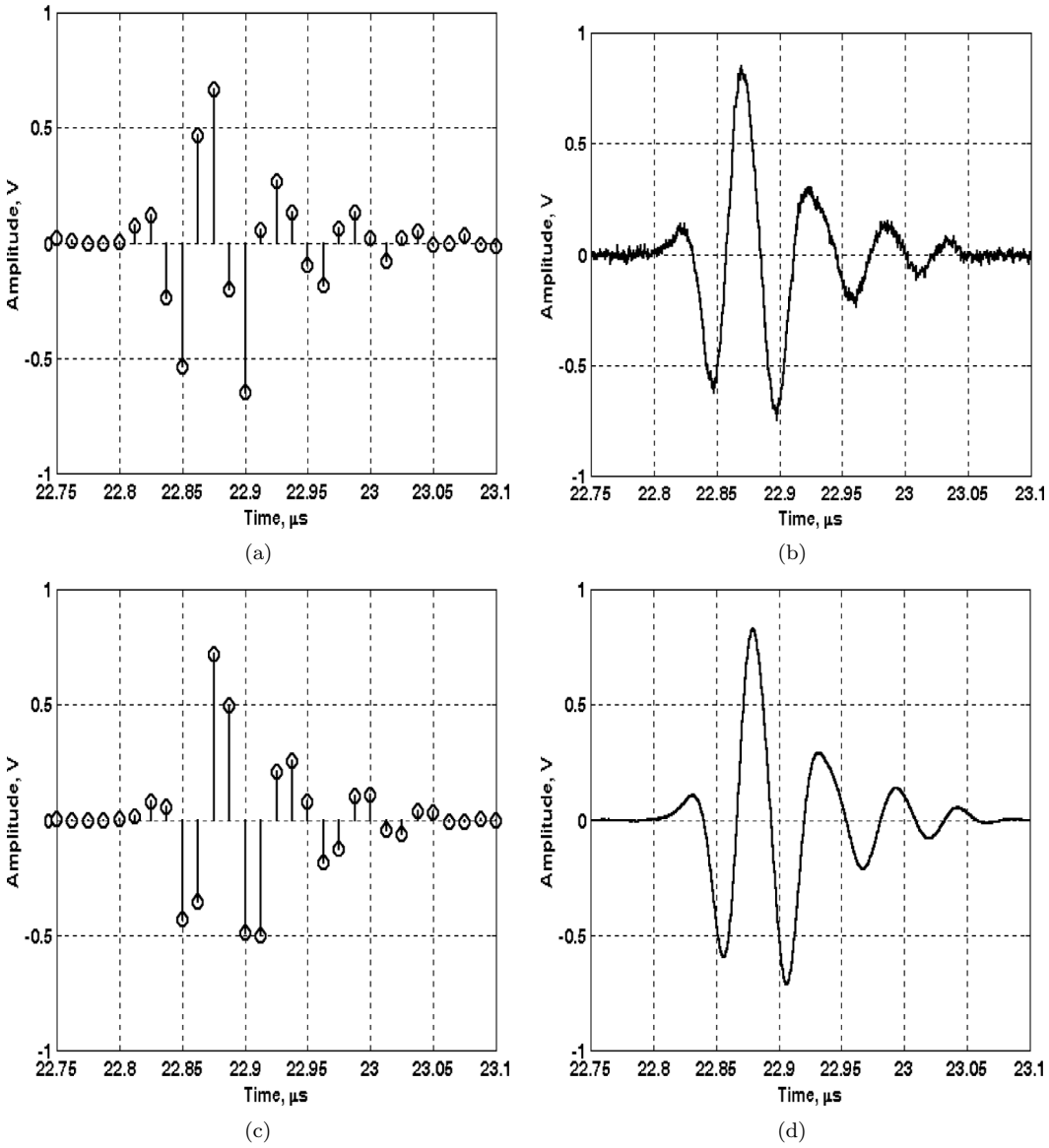

Fig. 9. Responses of a 20-MHz transducer recorded with different numbers of averages and sampling frequencies: (a) 2 averages, 80 MHz; (b) 2 averages, 2160 MHz; (c) 512 averages, 80 MHz; (d) 512 averages, 2160 MHz.

$$N_3 \mod (m-1) = 0. \tag{7}$$

When CONTROL 1 is enabled, it invokes sampling at the frequency f_1. This block generates the RAM address that is incremented by N_5 for each sample and is reset to zero when the block is disabled. The rest of the block diagram is the same as in Fig. 2 and operates in exactly the same manner as before and is thus not shown in Fig. 6. Every single record is completed in N_5 frames, and N_4 completed records are used for averaging. This results in the time required for measurements:

$$t_m = \frac{N_3 \times N_4 \times N_5}{f_2} = \frac{N_5 \times N_4}{f_{\text{exc}}}, \tag{8}$$

where f_{exc} is the excitation frequency ($f_{\text{exc}} = f_2/N_3$).

Successful operation of this design relies on the stability of the relation between the two clocks used. This stability is achieved by using a deep reset of DCMs before measurements that ensures proper locking of the phase-locked loop controlling the DCMs. The acquisition time of a single record depends on the pulse repetition rate, number of averages, and the clock ratio. It was observed experimentally on a number of occasions that this time does not need to be higher than a few seconds, and the short-term stability of the master clock was found appropriate. Using a dedicated state machine that detected an instant of close coincidence of these pulses, and enabled the acquisition ensured the synchronization of the phases of the two clocks.

VI. Overall Implementation of the Research Platform and Its Use

Fast prototyping tools are required for economic implementation of this type of architecture and so the design

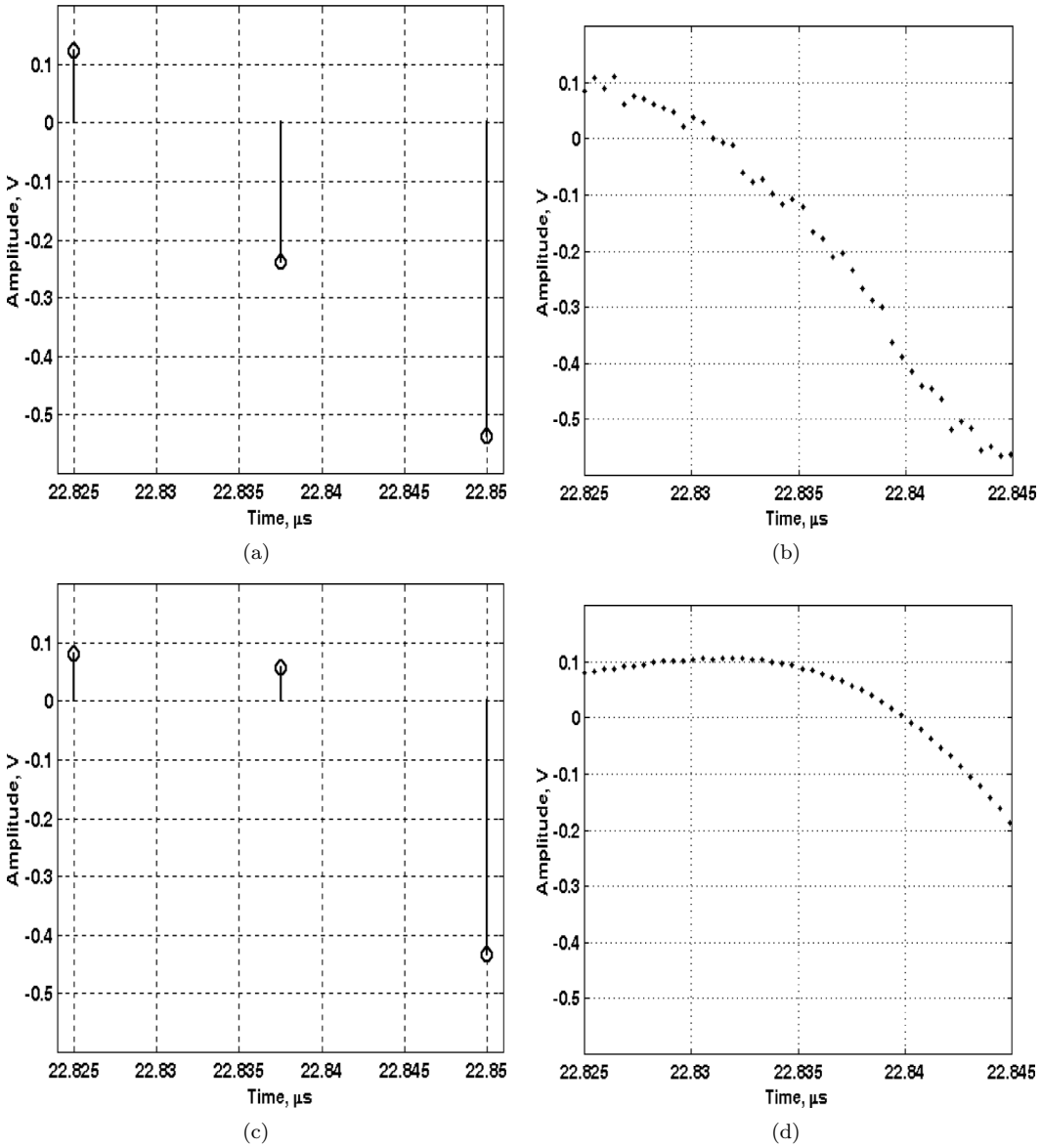

Fig. 10. A region around the first zero crossing of the responses of a 20-MHz transducer recorded with different numbers of averages and sampling frequencies: (a) 2 averages, 80 MHz; (b) 2 averages, 2160 MHz; (c) 512 averages, 80 MHz; (d) 512 averages, 2160 MHz.

package should support a high level of abstraction, design verification protocols, and convenient external interfaces. All of these requirements were met by the Xilinx Xtreme DSP development kit, which included the following relevant hardware:

- two 14-bit ADCs with a rated sampling frequency of 65 Msps,
- two 14-bit DACs with a sampling rate of 160 Msps,
- Virtex-II FPGA chip containing 3,000,000 logic gates.

The kit includes System Generator software that is a plug-in facility for the MATLAB Simulink toolbox. It provides a library of optimized components (for example, dual-port RAMs) and ensures simulation of the design both in software alone and also in co-simulation with hardware; it also allows easy data exchange between the development board and the MATLAB environment. The System Generator translates a high-level block diagram into a VHDL code that is subsequently converted in the FPGA bitstream. This feature allows integration of a custom VHDL code into the design and vice versa. The development kit was complemented by an ultrasonic pulser-receiver system (NDT Solutions Ltd., Chesterfield, UK) that provided the ultrasonic hardware front-end (Fig. 8).

Before arriving at our final design, we investigated a number of possibilities, some of which were successful and some of which were not, and in order to inform designers who may have an interest in related systems, we include some of these aspects here. High-speed averaging in hardware was straightforward but increasing the sampling rate was more difficult. It was possible to over-clock the on-board ADCs at up to 90 MHz instead of their rated 65 MHz without notable distortions of the acquired waveforms. The System Generator could not synthesize even simple circuits clocked above 120 MHz, even though the

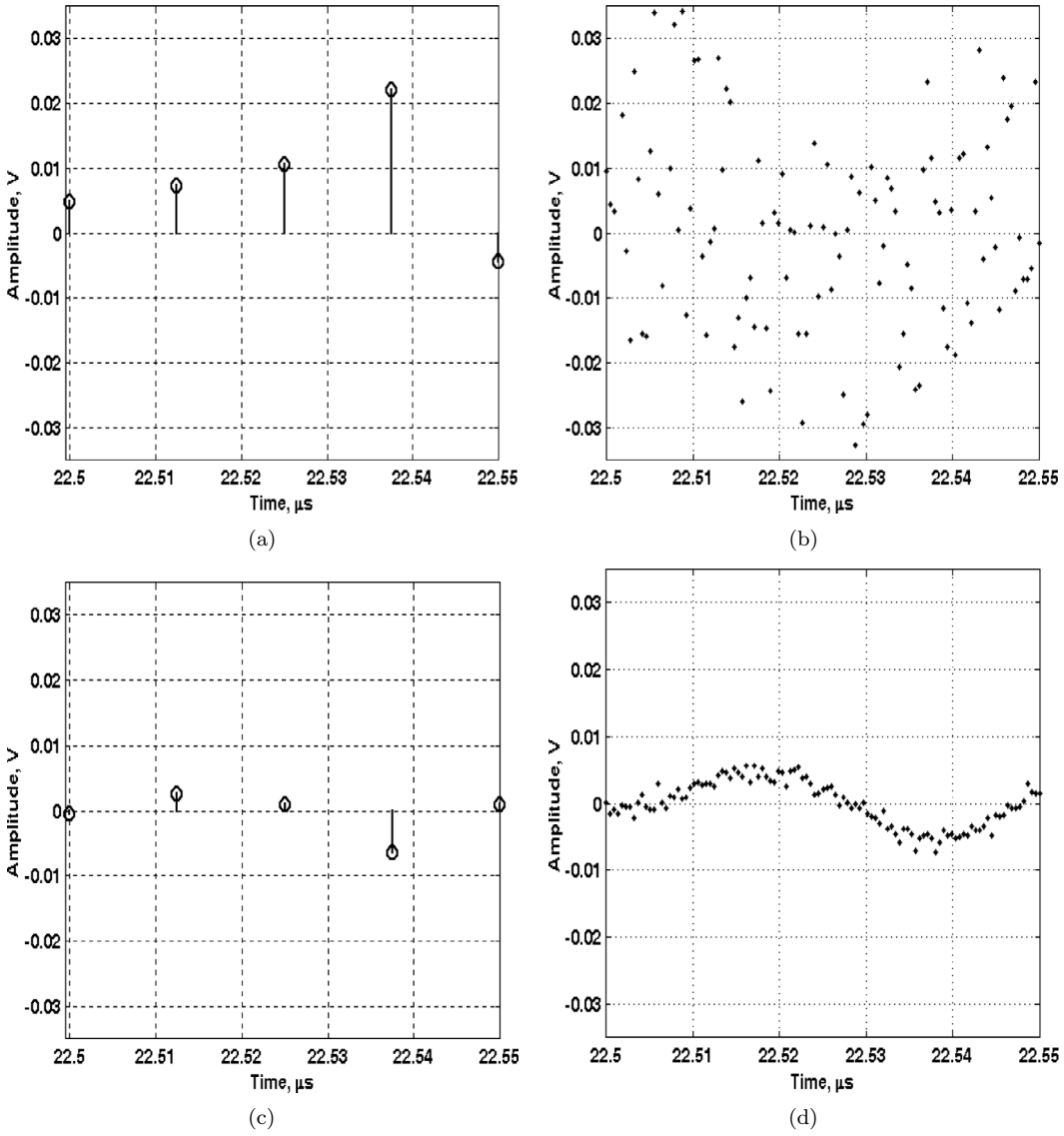

Fig. 11. A part of the overall signal record that contains supposedly the noise only: (a) 2 averages, 80 MHz; (b) 2 averages, 2160 MHz; (c) 512 averages, 80 MHz; (d) 512 averages, 2160 MHz.

rated clock frequency of the FPGA was 420 MHz. Because of this we were motivated to develop the two-clock architecture, although here the System Generator could not control the on-chip DCMs mentioned earlier. This problem was overcome by linking the System Generator output VHDL code to a custom VHDL code that was primarily intended for the control of DCMs. This code was subsequently imported as a black box back into the System Generator for use in both hardware co-simulation and the external computer interface.

The size of the dual-port RAM was the most restricting aspect of the system. At a 32-bit width, 16×1024 samples required in excess of 500 k bits and demanded much of the resource of the FPGA. This width is required to support up to 2^{18} averages for the 14-bit ADC used without a truncation, thus without any loss of accuracy. Key parameters for our system were up to $64 * 1024$ averages giving an improvement in SNR in excess of 40 dB where applicable, and a clock frequency ratio of 27:26 ($m = 27$) which gave an equivalent sampling rate of 2160 MHz with the ADC clocked at 80 MHz.

Examples of experimentally recorded ultrasonic signals are shown in Figs. 9–11 where the waveforms of interest are presented with different sampling frequencies (ADC sampling frequency of 80 MHz, and interleaved waveform with the equivalent sampling frequency of 2160 MHz, $m = 27$) and number of averages (2 and 512). These waveforms were obtained by using a 20-MHz transducer in water in the pulse-echo mode at a constant distance between the transducer and the reflector. The difference observed in the signal delays of the waveforms recorded with different numbers of averages was due to temperature changes in a test cell used. Fig. 9 shows the response of interest. Fig. 10 zooms into a region of the first zero crossing that is used for high-resolution estimation of delays of the ultrasonic pulses [1], [28], [29]. Fig. 11 presents an interval where the signal is supposedly absent. The comparison of the graphs shows that high-accuracy recording is possible

here by combining high-equivalent sampling frequency and a sufficient number of averages only (the bottom graphs on the right). The measurement time required for the waveform acquisitions was found to be equal to that determined by (8). At the pulse repetition frequency of 4 kHz, the measurement took 0.5 ms, 13.5 ms, 128 ms, and less than 3.5 s for the waveforms a, b, c, and d, respectively. The increase in the measurement time is the cost of the increase in accuracy.

High temporal resolution combined with the SNR enhancement improved the sensitivity of ultrasonic setups and their accuracy significantly on a number of occasions. First, the sensitivity of ultrasound to chemical changes that was previously demonstrated at a level of above 200 ppm [10] was improved several times, even for much less contrast reagents (publication pending). Second, the application of this research platform to the compensation of temperature changes led to the possibility of detecting 30 distinct readings for a change of the temperature of 0.1°C only [28]. Third, an application of the instrument to measurement of the linear dimension of steel samples of about 50 mm long showed an equivalent scatter of a few micrometers only that could lead to development of a novel online nondestructive process instrument for milling machines, etc.

Our most recent development included an addition of Golay code excitation. This addition affected both the excitation circuit and the memory controller as two different excitation sequences to be used, and the associated responses are to be stored separately.

VII. Conclusions

Advances in ultrasonic transducer technologies, and evolving challenges for new applications, are likely to be associated with requirements for higher data sampling rates and fast averaging for SNR enhancement. These will require new architectures for data acquisition systems and, ideally, these will be specified in a way that allows implementation on continually evolving development platforms, giving possibilities for future enhancement that is upwards compatible. The objective of this work was to achieve high-accuracy ultrasonic data acquisition with fast averaging combined with high sampling rates, both of which were implemented using contemporary FPGA technology. Averaging was best achieved using a hardware adder and a dual-port RAM, giving pipelined operation. A two-clock system provided for fast interleaved sampling implemented using the FPGA; it overcame the limitations of most commercial digitizers and had the distinct advantage that the system is portable to other FPGA platforms. It was compatible and easily integrated with the fast averaging system. The performance was excellent, sampling rates of 2160 MHz being achieved at very low cost. We believe that architectures such as ones we have described will provide the basis for future generations of ultrasonic instruments.

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