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Development of Electronic Components for an Integrated Ultrasonic Front End ASIC

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Abstract *– The development of an ASIC for ultrasonic front end is described. The ASIC contains a high speed binary driver and broadband amplifier optimised for a conventional piezoelectric transducer. Experimental results that agree well with simulations are presented and discussed.*

Keywords *– ultrasonic instrumentation, measurement ASIC, mixed signal ASIC*

I. INTRODUCTION

Ultrasonic measurements were proved as exceedingly effective in industry applications for non-destructive testing and in health services for various types of ultrasonic scans [1-2]. New arising ultrasonic applications and novel developments of high-frequency transducers define today's trend: higher operating frequencies to increase measurement resolution and use of arrays for imaging [3]. The former requires higher operating bandwidth, and the latter demands an integrated circuit (IC) solution to reduce off-chip interconnect. Designs based on non-integrated discrete components suffer from poor scalability and rather high costs [4-5]. Integrated solutions are intended to overcome abovementioned drawbacks. Some of these systems destined to minimise power consumption for battery operated devices, though this reduces achievable working frequencies [6-7]. Bandwidth of integrated designs is often limited to values up to 10-30 MHz [8-9] that reduces their usability for various ultrasonic measurement techniques.

Specialised front end based on custom integrated circuit with configurable wideband amplifier and excitation driver is capable to meet various combinations of desired features. Our goal was to implement the utmost flexible integrated cascadeable wide bandwidth amplifier and excitation driver with short transient response, both operating with piezoelectric transducers. Amplifier bandwidth should not be less than 50 MHz. The driver must provide rise/fall time of not more than 20 ns at 2 nF load which is typical for excitation of an ultrasonic transducer with central frequency up to 30 MHz. Such a front end is suitable for use in an ultrasonic integrated measurement system (e.g., [10]).

II. DESIGN PROCEDURES AND OUTCOMES

Low voltage excitation driver is required for advanced safety critical applications. Technology AMS 0.35 μm C35B4C3 was chosen for the front end ASIC as providing necessary 3.3V I/O voltage and timing parameters. Design routines were implemented using Cadence IC 5.0 software.

The driver stage is designed to be controlled by an external pulse source. In order to achieve good receiving conditions for the returned echo, the output transistors are automatically set to high impedance after the pulse has been sent – architecture [11] provides this feature. The rise/fall times of discharging and charging of the transducer were required to be 20 ns in line with foregoing explanation. This aim defines sizes of output driver's stage, as shown on final topology of the driver (fig.1).

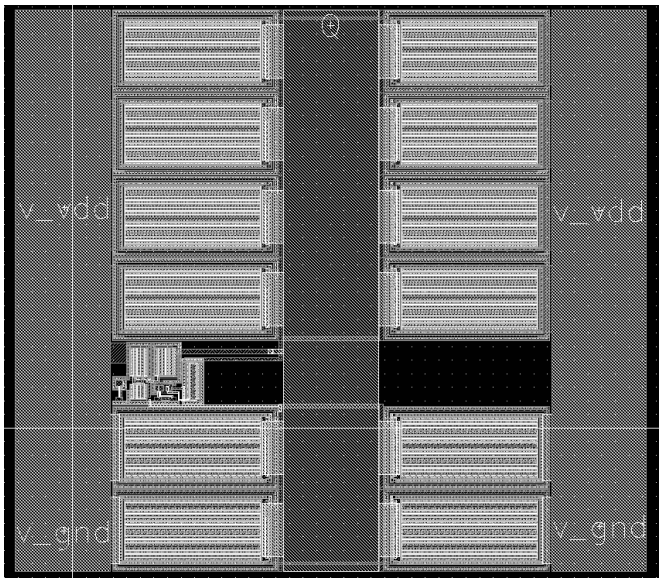

Fig.1. Design outcomes: excitation driver's layout

Possibility to adjust amplifier's gain was implemented by placing three identical op-amps and one cascaded amplifier comprising two op-amps connected in series on chip. Commutation of amplifiers provides variable gain values. We assessed the required bandwidth of the amplifier at 50 MHz for a 5 pF inter-chip stray loading capacitance. Amplifier [12] has been used with increased working currents providing higher driving capability. Simulation demonstrated 17 dB gain at 60 MHz bandwidth and 5 pF load, and 20 MHz with total 30 pF load, which is a realistic estimate for typical testing conditions when taping signal by an oscilloscope probe. Phase margin at 60 MHz was 60^o.

Noise is an important issue in sensor front ends. Effective number of bits equal to 10 over 2.4 V of output swing was the design goal. With a bandwidth of 50 MHz and gain of 17 dB this would require the equivalent input noise spectral density to be less than 23.7 $nV/\sqrt{Hz}$. Since the amplifier is supposed to work with different capacitive sources, this noise parameter is most crucial. Large input transistors (fig.2) provide low noises.

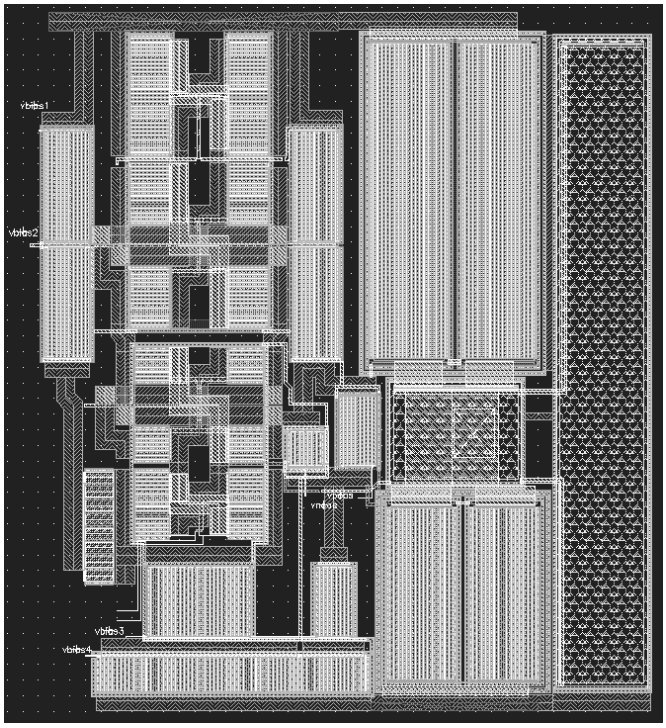

Fig.2. Design outcomes: amplifier's layout

Simulation of the amplifier confirmed that noise does not exceed this value within 0.35-60MHz (fig.3).

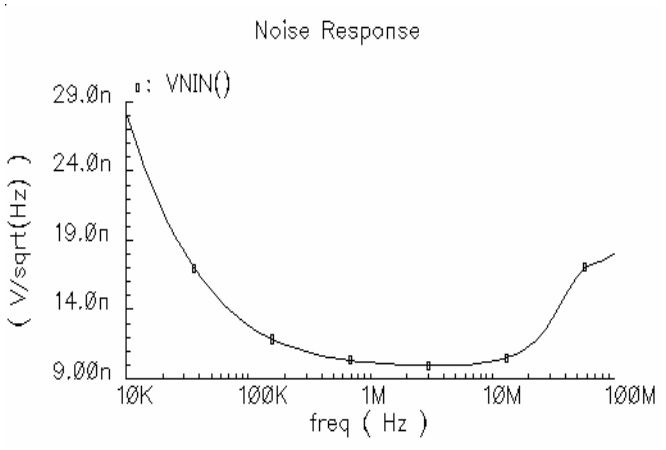

Fig.3. Simulation of amplifier's noise spectral density

The designed front end circuitry was put on a shared die, and the complete ASIC was packaged in PLCC-84 (fig.4).

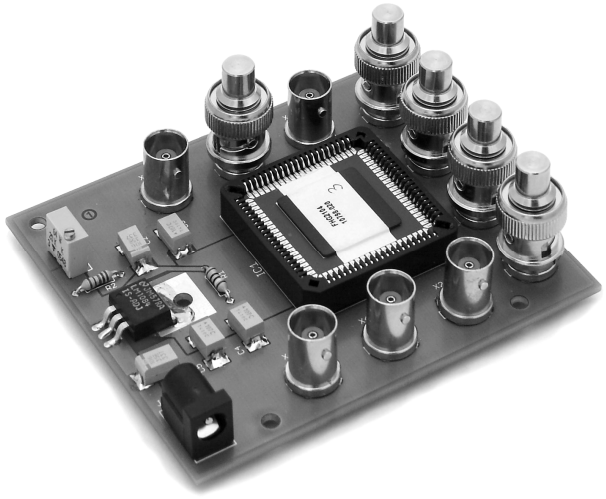

Fig.4. Design outcomes: ultrasonic pulser - receiver PCB utilising the designed front end ASIC

III. EXPERIMENTAL VERIFICATION

A. Components characterization

Testing of 5 fabricated chips demonstrated good uniformity of drivers and amplifiers parameters with discrepancy in range of few percents. The pulser-receiver PCB was implemented (fig.4) in order to test the front-end ASIC and to build an ultrasonic measurement system. Signal generator Advance Electronics B4A7 and digital storage oscilloscope LeCroy 9410 were used for characterization.

Testing the driver with 50 Ohm load by applying 50 ns 1V input pulses exhibited 20-30 ns rise and fall time (fig.5). The driver loaded by a piezoelectric transducer provided good attenuation of transients due to its low output impedance whilst switching (fig.6).

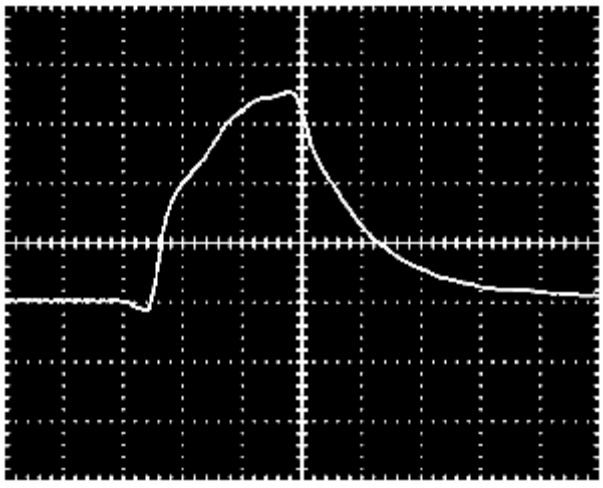

Fig.5. Excitation driver response for 50 ns pulse with 50 Ohm load, Scale: ordinate axis - 0.5V/div, abscissa axis - 20ns/div

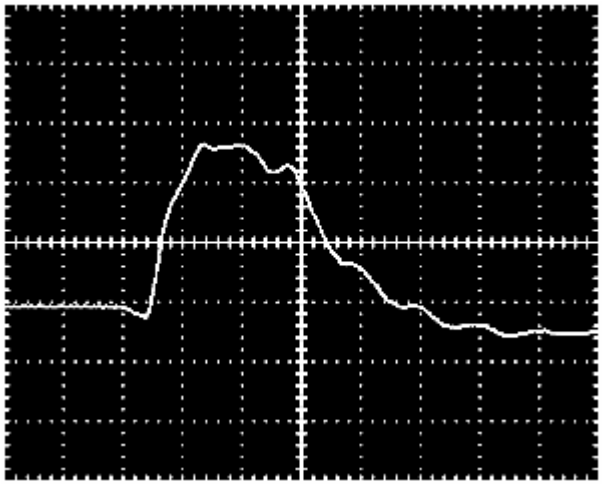

Fig.6. The excitation driver response for a 50 ns pulse measured at a Panametrics V317 20MHz transducer load,
Scale: ordinate axis - 0.5V/div, abscissa axis - 20ns/div

Comparison of simulated and measured bandwidths for single and cascaded amplifiers is shown in fig.7 and fig.8 respectively, where a good agreement can be seen.

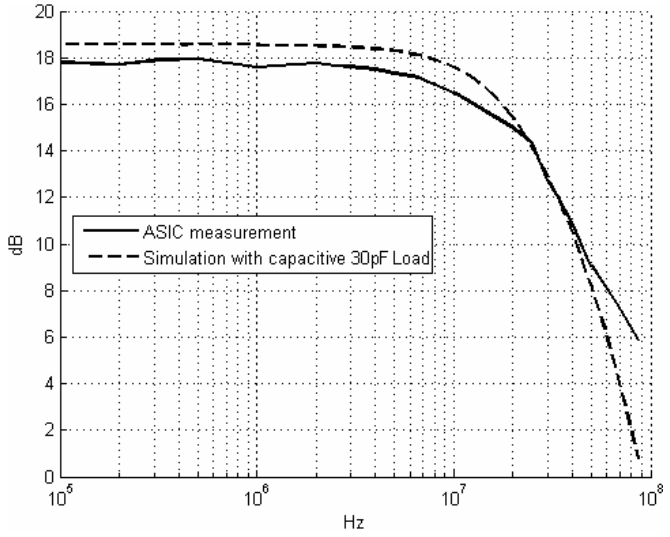

Fig.7. Comparison of experimental and simulated bandwidths of single amplifier

In both cases amplifier was loaded by 30 pF. Testing the cascaded amplifiers proved low scatter of their output DC bias that a provides convenient way to gain control by connecting several op-amps in series.

Measurement of the equivalent input noise spectral density gave value of 18.74 $nV/\sqrt{Hz}$ that satisfies the design requirements.

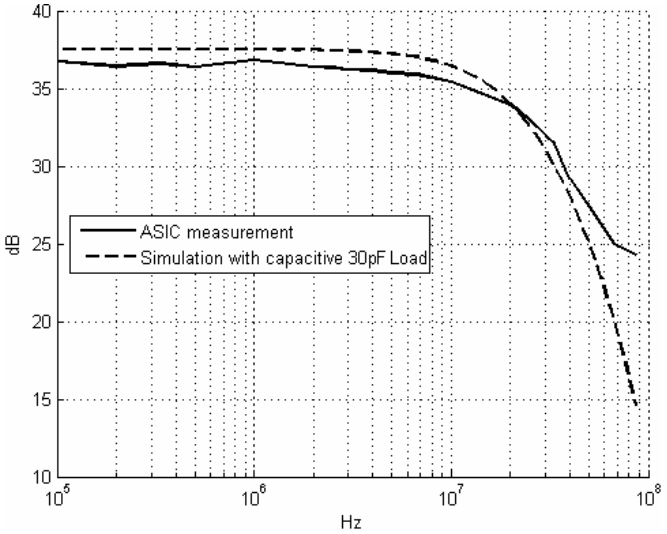

Fig.8. Comparison of experimental and simulated bandwidths of cascaded amplifier

B. Testing of ultrasonic pulser - receiver component

The designed front end ASIC was aimed to operate in typical ultrasound interrogating configurations: through and pulse-echo (fig. 9 and fig. 10 respectively).

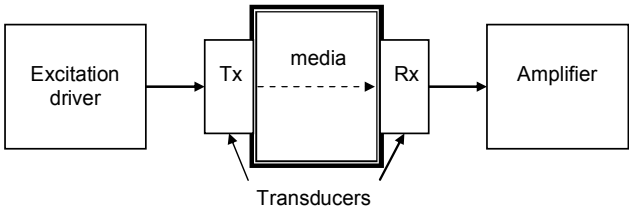

Fig.9. Through pulse test configuration

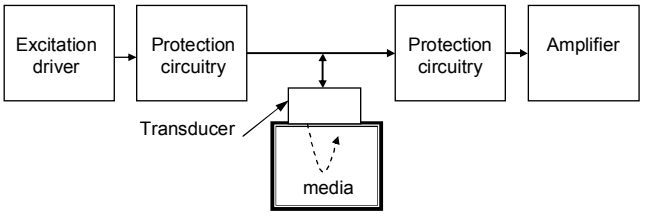

Fig.10. Pulse-echo test configuration

Test waveform obtained with a single amplifier in through pulse mode is presented in fig. 11. This test setup utilized two Panametrics V303 transducers with a central frequency of 10 MHz. A cascaded amplifier's configuration has been tested in the same environment. Resulting waveform is shown in fig. 12.

The most important feature of the designed front end is its capability to function in the pulse-echo mode. This requires protection of the amplifier from the excitation pulse (fig. 10).

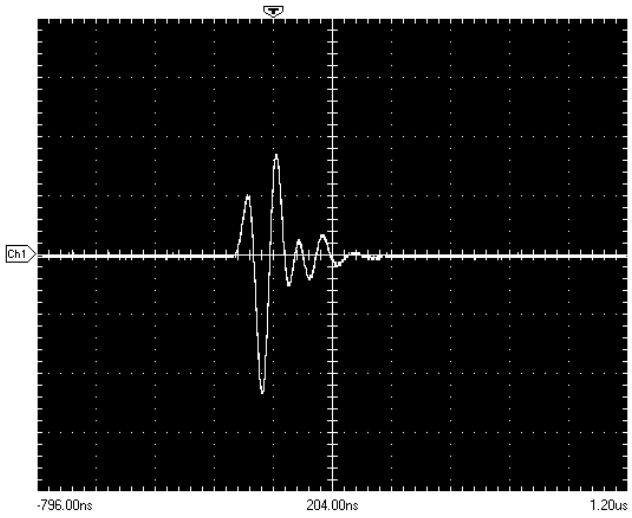

Fig.11. Pulse response acquired in through pulse mode with single amplifier,
Scale: ordinate axis - 100mV/div, abscissa axis - 200ns/div

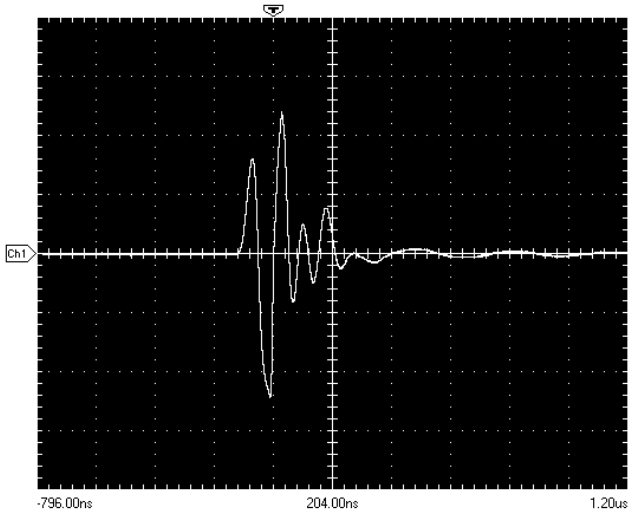

Fig.12. Pulse response acquired in through pulse mode with cascaded amplifier,
Scale: ordinate axis - 500mV/div, abscissa axis - 200ns/div

For the pulse-echo mode the protection of input amplifiers from a high-voltage excitation circuitry is provided by diode bridges, transformers, or high-voltage switches. These solutions make ultrasonic equipment expensive, bulky, and power consuming. Moreover these additional components contribute an extra input noise thus reducing a signal to noise ratio.

The implemented low voltage excitation circuitry and use of Electrostatic Discharge (ESD) protection embedded in ASIC I/O pads (fig. 13) eliminate a need for additional protection circuitry. This sort of protection simplifies interconnect for transducer arrays as an added advantage.

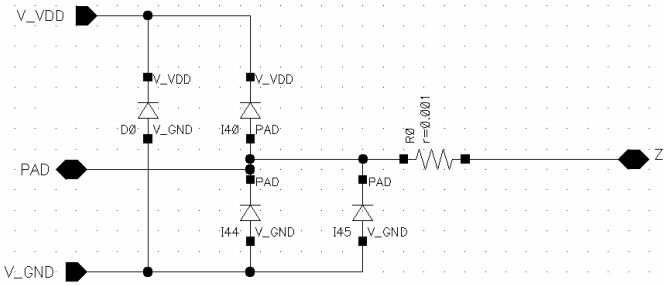

Fig.13. Schematic of utilized I/O pads with ESD protection

This approach was tested using a setup presented in fig.14.

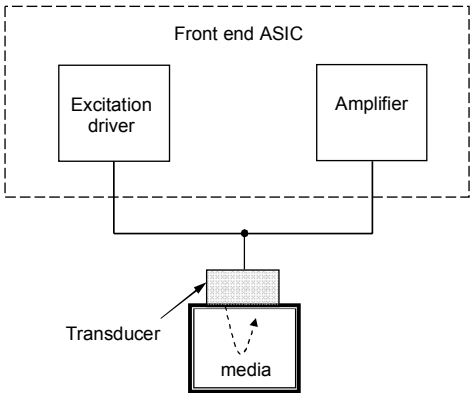

Fig.14. Setup for testing of front end ASIC in pulse-echo mode

The measured waveforms for single and cascaded amplifier configurations are shown in fig. 15 and fig. 16 respectively. Bigger pulse (at the left side) corresponds to the excitation pulse induced to the amplifier stage. In particular, it contains an excitation pulse itself and a power surge resulted from limited conductivity of power buses in the ASIC.

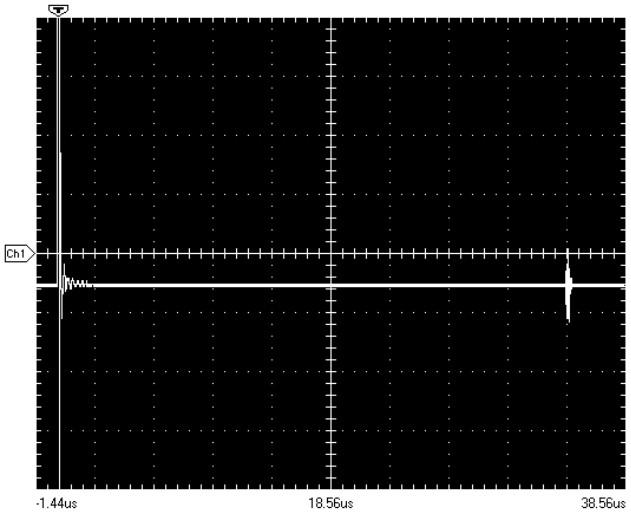

Fig.15. Recorded waveform for a single amplifier,
Scale: ordinate axis - 100mV/div, abscissa axis - 4µs/div

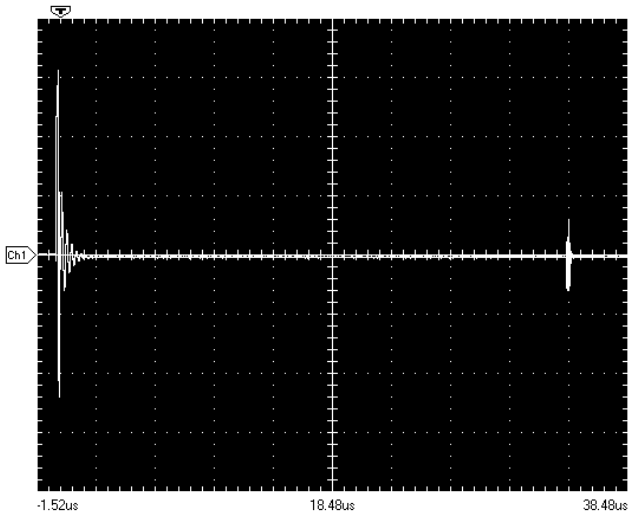

Fig.16. Recorded waveform for cascaded amplifier,
Scale: ordinate axis - 500mV/div, abscissa axis - 4µs/div

Ringing after excitation pulse lasts in range of 2-3 µs, which is suitable for most ultrasonic testing methods. Transient process can be noticeably shortened if connection between a transmitting driver and an input amplifier will be implemented inside an ASIC.

Power surge induced by the excitation pulse is visible even in a through pulse configuration (fig. 18 on the left). Its amplitude is several times lower than that of the signal of interest in the pulse-echo mode, and can be neglected in most cases. Further reduction of this voltage can be achieved by implementing separate power supplies for amplifiers and drivers.

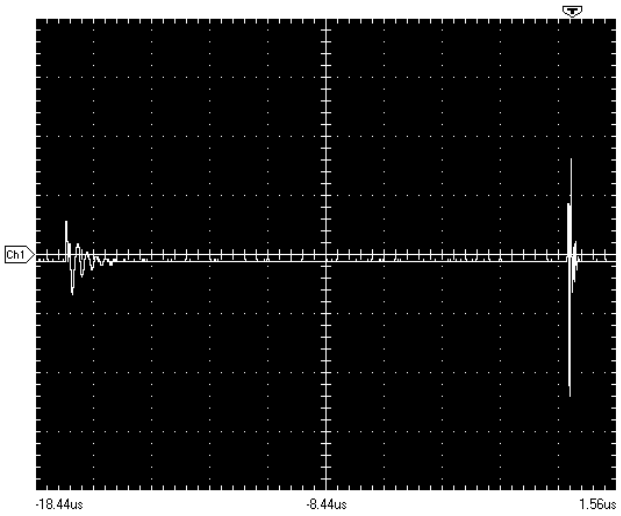

Fig.18. Power surge induced by the excitation pulse to the output of the single amplifier (left pulse) visible in the through pulse mode,
Scale: ordinate axis - 100mV/div, abscissa axis - 2µs/div

IV. SUMMARY AND CONCLUSION

Elements of the front end of an ultrasonic instrument were successfully designed, manufactured and tested. Implemented excitation driver provided rise and fall time in range of 20-30 ns with a 2 nF load typical for ultrasonic transducers. The amplifier showed gain of 17-18 dB and a bandwidth from 20 MHz (with a 30 pF load) to 60 MHz (with 5 pF load). Doubling the gain was achieved by connecting two op-amps in series on die. All components operated stably with a supply voltage in a range of 1.24 V- 3.5 V.

The front end was tested in typical setups for ultrasonic measurements. It provided functionality of two modes: through pulse and pulse-echo. It has been shown that architecture with low voltage excitation does not require additional protection circuitry to isolate input amplifiers from the excitation pulse and following transient spikes. This can significantly simplify design of equipment for advanced safety critical applications.

Next step in our development is to implement complete integrated ultrasonic front end ASIC with a digital supervisory control.

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