High-Speed Digitizing of Repetitive Waveforms Using Accurate Interleaved Sampling

Vladimir G. Ivchenko, *Member, IEEE*, Alexander N. Kalashnikov, *Member, IEEE*, Richard E. Challis, and Barrie R. Hayes-Gill

***Abstract*—Random interleaved sampling has become a widespread operating mode for digital storage oscilloscopes. Different repetitions of (notionally) the same waveform are recorded at random time shifts and are interleaved in memory, resulting in an increase of the equivalent sampling frequency. This procedure requires substantial time, particularly if further averaging is required. In this paper, an approach that ensures accurate time shifts is presented for repeated waveform measurements. Operating two independent oscillators with related frequencies forms the accurate shifts. One of these is used to excite a waveform of interest repeatedly, and the other clocks the analog-to-digital converter (ADC). This architecture was implemented using a commercial "off-the-shelf" field programmable gate array. Examples of experimental waveforms, which are sampled at 2160 MHz using an ADC that is clocked at 80 MHz, are presented. They are compared with the simulated and independently measured waveforms where appropriate.**

***Index Terms*—Accurate interleaved sampling (AIS), repetitive excitation, two clock timing architecture, ultrasonic instrumentation, waveform measurement.**

I. Introduction

HIGH-SPEED digitizing of waveforms of interest plays an important part in broadband communications and electronic measurements. While the former application deals with an information-carrying waveform that is available once only, the measured waveform could be excited at will many times. For example, repetitive excitation of the test signal is a conventional mode of operation for ultrasonic imaging instruments to achieve the additive noise reduction by coherent averaging.

Ultrasonic imaging techniques are well established in medical diagnostics, flaw detection, and imaging in the context of large engineering structures [1]. Applications of ultrasound to material evaluation are also well established, and there is a growing interest in the use of similar methods to monitor chemical phenomena both in the laboratory and in process [1], [2]. The traditional approach in digitizing ultrasonic waveforms using a single high-speed analog-to-digital converter (ADC) becomes nonviable for novel transducers/systems operating at above 100 MHz because of the high cost involved and specific expertise required. Numerous examples of these applications are presented every year, which are based either on laser ultrasound, cMUT, or pVDF devices [3]. This requires further development of alternative architectures for high-speed digitizing in ultrasonic instruments.

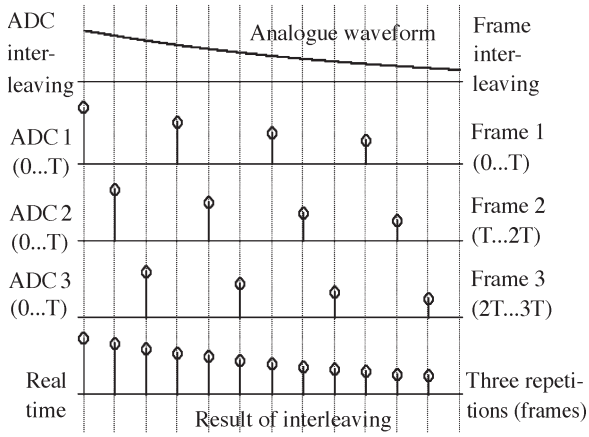

Fig. 1. Threefold interleaving (on the left—ADC interleaving; on the right—AIS interleaving).

Interleaving presents an architectural possibility of improving the equivalent sampling frequency of data acquisition system by up to an order of magnitude and more. A great deal of attention is paid at the moment to the development and analysis of systems containing several ADCs that substitute a single high-speed ADC operating in real time (e.g., [4] and [5], Fig. 1, captions on the left). The inherent disadvantages of this approach are the increase in cost of components and their interconnection compared to a single low-speed ADC and analysis/prevention/compensation for inaccuracies appearing due to differences in parameters of different ADCs used. In spite of these, ADC interleaving could be cost effective or even the only possible solution in sampling nonrepetitive waveforms due to the high cost or unavailability of a single ADC solution.

Both disadvantages of ADC interleaving could be avoided if the sampled waveform is repetitive (or can be excited repeatedly). In this case, a single low-speed ADC can be employed for different repetitions (frames) of the waveform of interest with different time offsets, resembling ADC interleaving (Fig. 1). The inherent disadvantage here is the inability to sample nonrepetitive waveforms (e.g., communication signals) in real time. However, for some applications like wave remote sensing (e.g., ultrasonic NDE/NDT, active radar and sonar imaging, and range finding), it is possible to excite (notionally) the same

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waveforms over and over again if the repetition frequency is relatively high and/or movement of targets is relatively slow.

Frame interleaving is often used to improve temporal resolution of digital storage oscilloscopes (DSOs). Random interleaved sampling (RIS) involves digitizing several waveforms, accurate measurement of a time difference between an external trigger event and the nearest edge of an internal DSO ADC clock, and interleaving the acquired waveforms according to their position in the time domain [6]. The disadvantage of the method becomes evident if high-resolution acquisition is required and/or averaging is involved. In this case, a complete acquisition requires a significant amount of time due to inherent randomness of the RIS. On the other hand, if the waveform of interest can be excited at will, it is possible to achieve a small frame jitter for the acquired waveform [7] and employ accurate interleaved sampling (AIS). The number of frames required to complete the acquisition would be exactly equal to the interleaving factor (Fig. 1)—a significant advantage over the RIS. The price AIS pays for the increase in temporal resolution comparing to ADC interleaving, or a single ADC is the proportional increase in measurement time.

AIS, in principle, could be implemented by using a multiphase clock oscillator designed for ADC interleaving. Unfortunately, existing application-specific integrated circuits remain proprietary (e.g., [8]). Building these oscillators from digital electronic components would require high internal clock frequencies, which rules out convenient commercially available reconfigurable logic devices. The aim of our development was to implement scalable AIS using commercially available field programmable gate arrays (FPGAs).

An additional advantage of interleaving is a reduction in power consumption compared to a single ADC [9, Sec. 4].

This paper describes the results of developing a frame interleaved AIS data acquisition architecture for an ultrasonic instrument and its implementation using commercially available FPGA technology and design tools and presents examples of acquired waveforms that were verified by simulations and independent measurements.

II. Using Two Oscillators With Related Frequencies for Accurate Timing

Let us consider two oscillators whose frequencies precisely satisfy the following relationship:

$$M_1 f_1 = M_2 f_2 \tag{1}$$

where $M_1 \in N$, $M_2 \in N$, and $M_1 = M_2 + 1$. This condition implies that if the rising edges of the oscillators coincided at some instant t_0, they would exactly coincide again at

$$t_k = t_0 + k\frac{M_1}{f_2} = t_0 + k\frac{M_2}{f_1}, \qquad k \in N. \tag{2}$$

It makes it possible to predict when the oscillators will have their rising edges coincident again by counting their pulses to M_1 (for f_2) and to M_2 (for f_1). By using one clock sequence for excitation and the other for sampling, it is possible to acquire exactly the same waveforms many times for any integer values of k in (2).

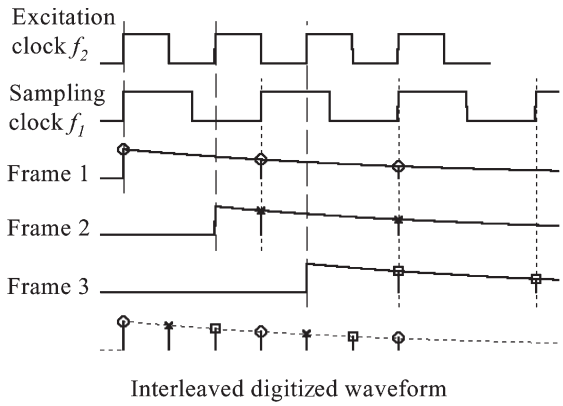

Fig. 2. Operation of two clock architecture for the clock ratio of 2 : 3 (Dashed lines: excitation of a particular frame; dotted lines: sampling instants).

Two-clock timing architecture assumes that the first repetition (frame) will be excited when the rising edges of both clocks coincide, but the following waveforms will be excited by the successive pulses. This is illustrated in Fig. 2 for sampling an exponentially decaying pulse stimulated by different successive rising edges of clock f_2. At the first repetition of the excitation, the edges of the clocks coincide with each other (frame 1, Fig. 2). The first pulse of f_2, as shown in Fig. 2, triggers the excitation. The ADC samples an input signal with zero delay relative to the edge of the excitation pulse. The successive repetitions should be delayed by a time interval that satisfies (2) to ensure coherence and is large enough for the measured waveform from the previous excitation to decay to zero. These delays are omitted in Fig. 2 for clarity of the picture. At the second repetition, the excitation trigger is associated with the second pulse of f_2. The ADC starts sampling after the excitation trigger from the second pulse of f_1. This ensures a delay between the excitation and the sampling sequence of $1/f_1 - 1/f_2$ (frame 2). At the third repetition, the third pulse of f_2 triggers the excitation pulse. The ADC is clocked with the delay of $2 \times (1/f_1 - 1/f_2)$ to the excitation trigger, that is, frame 3. The acquired samples are interleaved in RAM, and the RAM address is incremented by M_1 (rather than one) for every successive sample in the same frame; the addresses in every successive frame are offset from the previous frame by one. After the acquisition of the last frame (third frame in Fig. 2), this offset is reset to zero. The acquisition, therefore, could continue from frame 1 synchronously, thereby enabling, if desirable, coherent averaging [10]. Coherent averaging is routinely used in ultrasonic measurements to reduce the uncertainty of the acquired data (e.g., [11]).

Two clock sampling architecture is employed for the acquisition of a single sample per frame only in on-chip oscilloscopes [12]. This limits the application of the technique to cases where few samples are to be collected at high repetition rates. For example, the ultrasonic signal presented in Fig. 3 consists of 2160 samples for 1 μs at the equivalent sampling frequency of 2160 MHz. The signal could be excited at a maximum repetition frequency of 4 kHz in order to avoid unwanted reflections (e.g., [11]) in the test medium that otherwise could overlap the response of interest. A single record without averaging required a measurement time of 27/4 kHz $<$ 7 ms in our system,

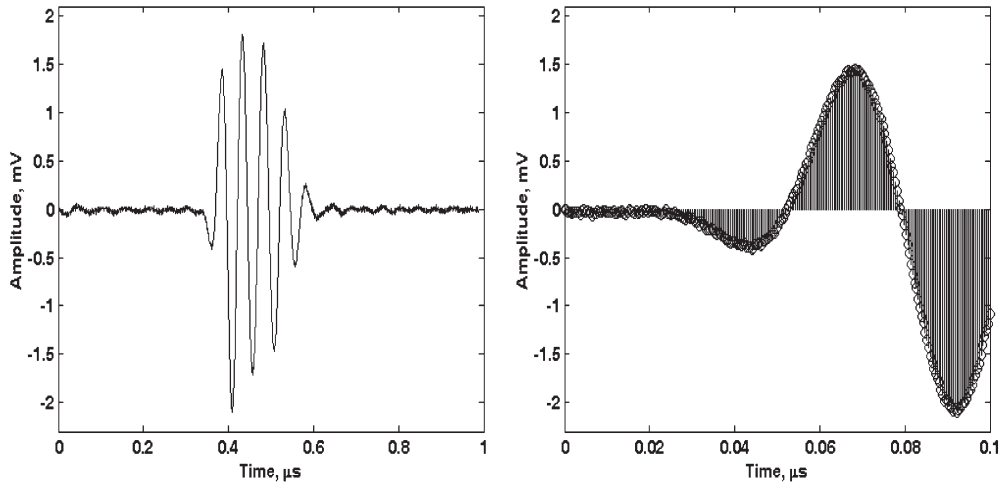

Fig. 3. Experimentally recorded ultrasonic signal (clock ratio of 26/27, ADC frequency of 80 MHz, equivalent sampling frequency $27 * 80 = 2160$ MHz, 1024 averages, and transducer central frequency of 20 MHz).

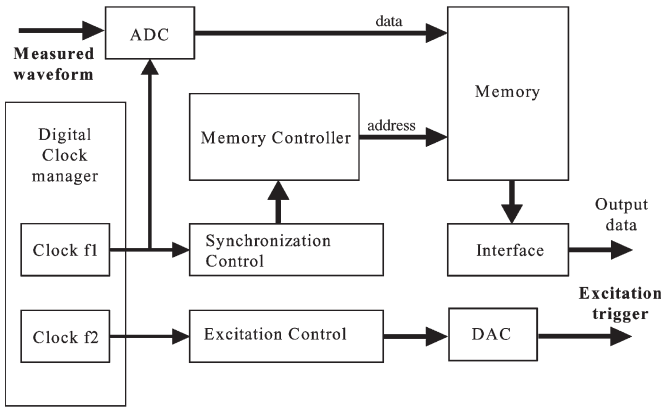

Fig. 4. Block diagram of two-clock timing architecture.

while using a single sample per frame technique would require $2160/4$ kHz $= 540$ ms. Getting 1024 averages, as in Fig. 4, would require more than 540 s for the on-chip oscilloscope, while in our system, it took less than 2 s.

III. Implementation of Two-Clock Architecture

The very close synchronization that is required in this system can be achieved, for example, by using digital clock managers (DCMs) available on Xilinx FPGA chips. These DCMs are capable of generating several related and tightly synchronized clock sequences. The ADC (lower frequency, f_1) is clocked by the basic frequency obtained from an on-board low jitter oscillator, while the excitation trigger (higher frequency, f_2) is clocked by a synthesized signal, which is synchronized with the basic frequency and produced by the DCM.

Fast prototyping tools are required for economic implementation of this type of architecture, and therefore, the design package should support a high level of abstraction, design verification features, and convenient external interfaces. To meet all of these requirements, the Xilinx Xtreme DSP development kit was used (Xilinx, San Jose, CA), which included the following relevant hardware: two 14-bit ADCs with a rated sampling frequency of 65 Msps, two 14-bit DACs with a sampling rate

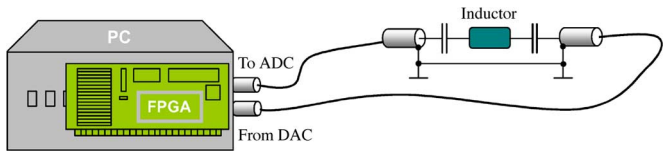

Fig. 5. Experimental setup.

of 160 Msps, and reconfigurable Virtex-II FPGA chip containing 3 million logic gates. The kit includes System Generator software that is a plug-in facility for the MATLAB Simulink toolbox. The development kit was complemented by an ultrasonic pulser-receiver system (NDT Solutions Ltd., Chesterfield, U.K.) that provided the ultrasonic hardware front-end.

Because the System Generator could not control the on-chip DCMs mentioned earlier, we linked the System Generator output very-high-speed integrated circuit (VHSIC) hardware description language (VHDL) code to a custom VHDL code that was primarily intended for the control of DCMs. The resulting code was subsequently imported as a black box back into the System Generator for use in hardware cosimulation. The block diagram of the design is presented in Fig. 4. Both acquisition and excitation parts of the design operate independently, although their internal parameters depend on the chosen clock ratio (hard coded) and repetition frequency (soft coded).

The size of the on-chip dual port RAM was the most restricting aspect of the system. At 32-bits width, 16×1024 samples were required in excess of 500k bits and demanded much of the resource of the FPGA. Key parameters for our system were a clock frequency ratio of 26/27, which gave an equivalent sampling rate of 2160 MHz with the single ADC clocked at 80 MHz and the accompanying feature of averaging if required.

The described instrument was used for various ultrasonic measurements (e.g., [10] and [13]).

IV. Verification of the AIS Design Operation

Waveform measurements are frequently required for experimental determination of responses of a linear device to particular stimuli, e.g., impulse and step responses. The operation of the designed AIS digitizer was verified by comparing the

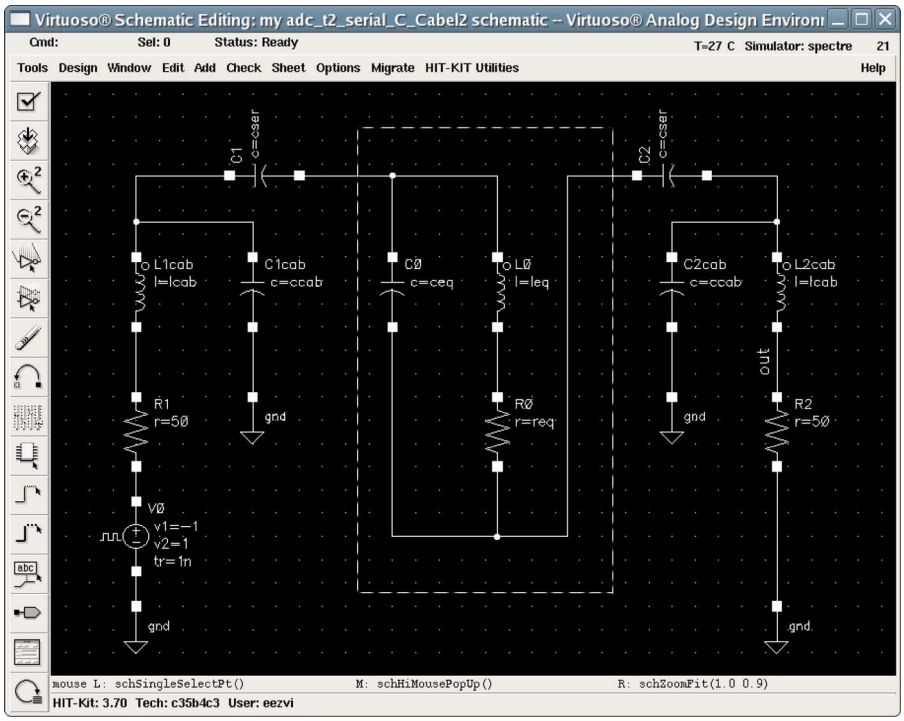

Fig. 6. Equivalent circuit of the experimental testbench (dashed line outlines the equivalent circuit for the inductor).

TABLE I
TEST SETUPS

	SMD inductor itself				Capacitors	Simulated resonant frequency, MHz	
	(lec), nH	(ceq), pF	(rec), Ohm	resonant freq, MHz	(cser), pF	Without cable	With cable
Setup1 Inductor Panasonic ELJFA5R6JFN	5600	1.81	1.6	50	68	11.2	11.2
Setup2 Inductor Panasonic ELJNDR33JF	330	1.9	2.16	200	10	106	46

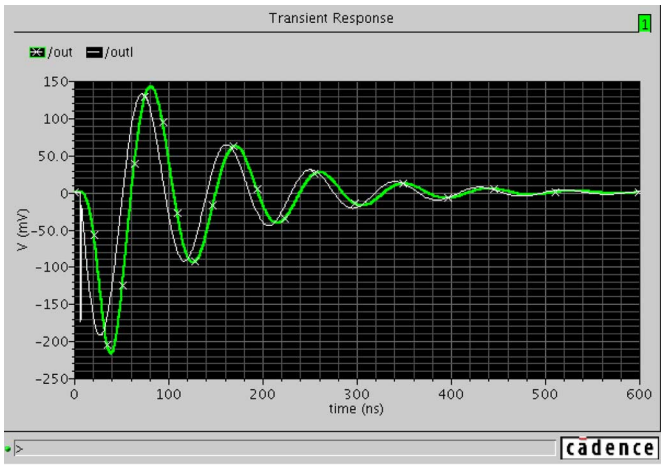

Fig. 7. Simulation results for setup 1 (/out—crossed line: simulation with lumped components representing the cables; /outl plain line: simulation without inclusion of the cables).

experimental waveforms with those obtained by simulation using Cadence Virtuoso Spectre circuit simulator [14] and measured by a conventional DSO (LeCroy 9314CM [15]).

The experimental setup consists of a serial LC circuit connected to the on-board DAC of the Xtreme DSP board (falling edge step excitation of 2 V p-p was used) and ADC by two coaxial RG316 cables (Fig. 5). This setup was simulated by representing the cables as lumped components due to their short length of 1 m, as compared to the relevant electromagnetic wavelength (Fig. 6, ccab $= 96$ pF/m $\times$ 1 m $= 96$ pF, lcab $=$ 240 nH/m $\times$ 1 m $= 240$ nH). The total length of the cables (2 m) leads to reactances with the resonant frequency of about 46 MHz that could influence both simulations and measurements heavily. Table I lists the values used to achieve resonant frequencies of the series LC circuit that differ by about an order of a magnitude. The simulation of the setup 1 shows that the cables delay the excitation slightly but do not change the ringing frequency notably (Fig. 7, Table I). However, their influence dominated for setup 2 (Fig. 8, Table I).

Waveforms measured using both instruments for setup 1 are shown in Fig. 9 [Fig. 9(b) was obtained by using the rising edge of the step excitation for comparison. It resulted in an inversion of the waveform]. They display consistency with each other and simulations (Fig. 7). As for setup 2, both instruments confirmed the dominance of the cables, although there were differences in the shape and amplitude of the response (Fig. 10). This difference is attributed to the use of a conventional cable that connected the output of the test circuit to the 9314CM oscilloscope. The use of averaging required the measurement time of about 100 s for 500 averages for the

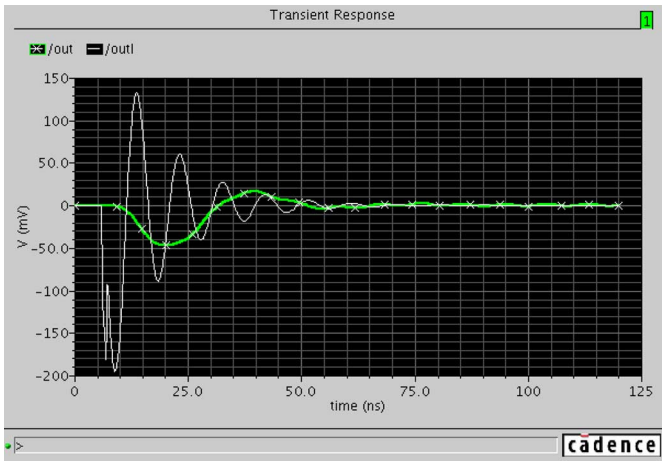

Fig. 8. Simulation results for setup 2 (/out—crossed line: simulation with lumped components representing the cables; /outl plain line: simulation without inclusion of the cables).

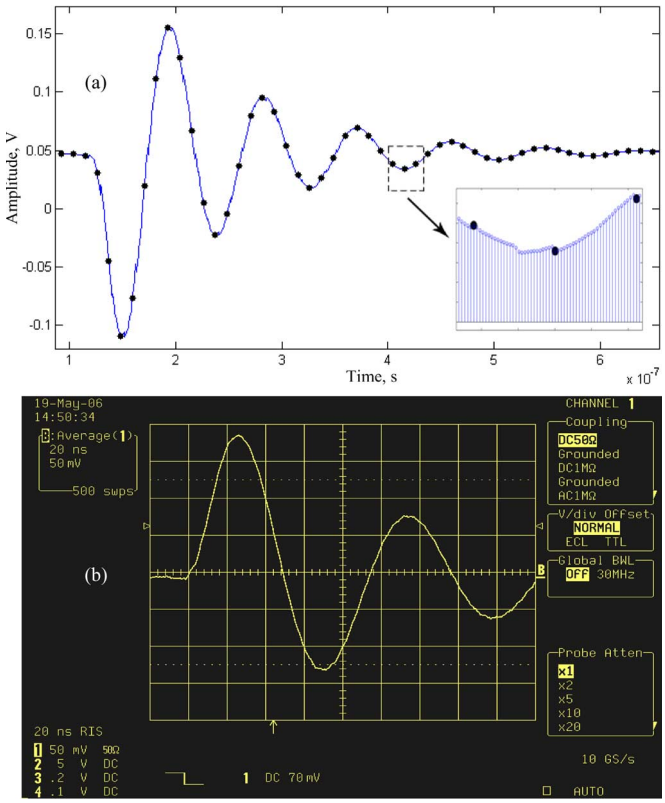

Fig. 9. Measured waveform for setup 1. (a) Acquired by the designed instrument; 512 averages; solid line represents the complete waveform, dots represent data acquired for a single frame only, and a zoomed fragment showed samples acquired by the AIS instrument. (b) RIS acquisition by the oscilloscope; 500 averages, and the waveform is inverted as the rising edge step excitation was used here for comparison.

9314CM oscilloscope, while the developed instrument completes 512 averages in less than 1.5 s due to on-the-fly averaging employed [10].

The difference in measurement times of two orders of magnitude was observed when a step response of the cables alone was measured without averaging. This seems reasonable, considering the difference in the acquisition mechanism of AIS versus

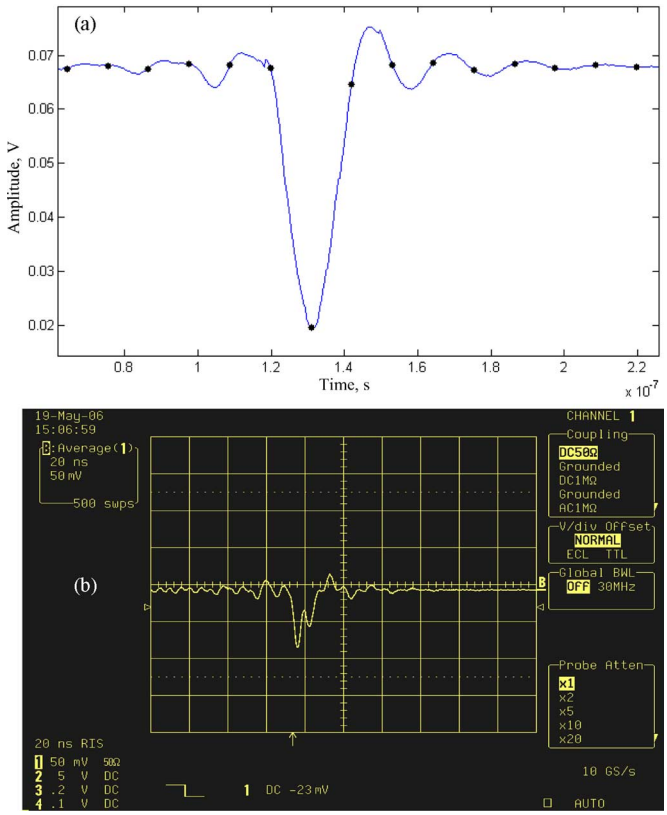

Fig. 10. Measured waveform for setup 2. (a) Acquired by the designed instrument; 512 averages; solid line represents the complete waveform, and dots represent a single frame. (b) RIS acquisition by the oscilloscope and 500 averages.

RIS. The AIS instrument provided a spurious free waveform, while the 9314CM oscilloscope recorded a distorted waveform (Fig. 11). It was observed that the occurrence of distortions was linked to the equivalent time-domain resolution of the RIS instrument (the higher it was set, the higher these occurrences were). These distortions might be linked to errors in evaluation of the actual delays during the RIS acquisition. If they are independent and random, their influence is equivalent to the influence of the frame jitter [7]. The later influence could be reduced by averaging [7], and this is a likely reason for the absence of distortions in the RIS averaged waveforms presented above (Figs. 9 and 10).

An important feature of the AIS waveform is the implicit presentation of the cable ringing at about a half of the ADC "native" sampling frequency. This ringing would be overlooked if the ADC clocked at 80 MHz was used without AIS, as shown by dots in Fig. 11.

V. Conclusion

Interleaving extends high-speed sampling capabilities of ADCs by an integer factor that equates to the number of ADCs used (ADC interleaving) or frames used (frame interleaving). Frame interleaving is applicable if the waveform of interest is (or could be made) repetitive. Interleaving leads to a lower power consumption when compared with a single high-speed ADC.

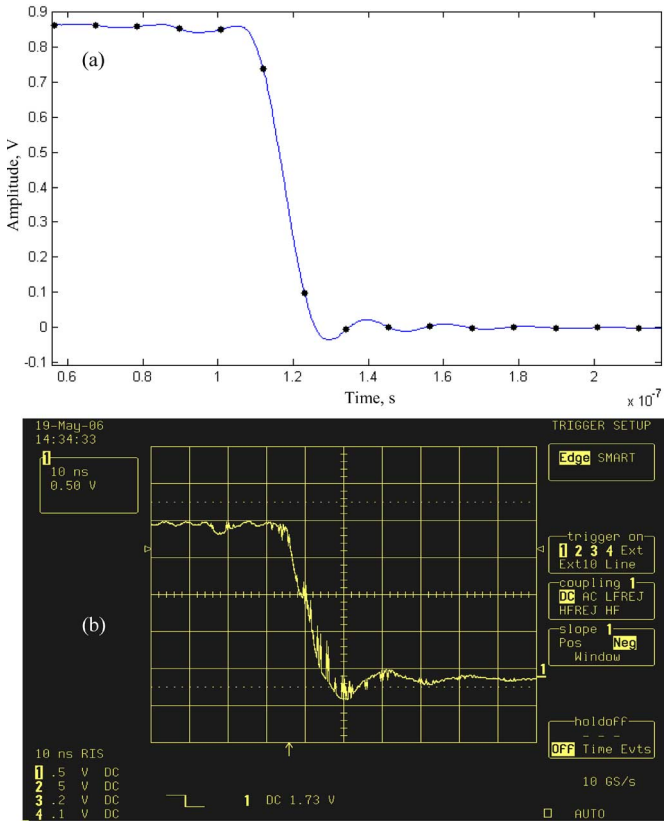

Fig. 11. Measured step response of the cables itself. (a) Acquired by the designed instrument; two averages; solid line represents the complete waveform, and dots represent a single frame. (b) RIS acquisition by the oscilloscope and no averaging.

RIS assumed independent sampling of repetitive signals and interleaving the acquired waveforms according to the time to trigger event measured separately. AIS employs generation of the trigger event tightly linked to the acquisition clock, providing as many precise equidistant time shifts from frame to frame as the interleaving factor required. Both ensure an increase in the equivalent sampling frequency at the expense of the measurement time required.

Two-clock architecture for AIS provides the required time shifts by using two tightly linked oscillators operating at different frequencies. It could be implemented using commercial off-the-shelf FPGA chips, which was illustrated by the use of the Xtreme DSP development kit. The added advantage of this architecture and its FPGA implementation is the compatibility with the on-the-fly averaging that reduces the overall measurement time (by two orders of magnitude in the considered case comparing to the RIS instrument used). The equivalent sampling frequency was increased by a factor of 27 when compared with the ADC clock frequency itself.

Simulations and independent measurements using a commercially available RIS oscilloscope verified the correct operation of the designed instrument. The AIS instrument showed significant advantages for both averaged (in terms of significantly reduced measurement time) and nonaveraged (absence of spurious distortions) waveforms.

Two-clock AIS architecture was developed primarily for use in ultrasonic instruments where the waveform of interest could be excited repeatedly at will. Some other applications that would benefit from the reported development include short-range radars and network analyzers.

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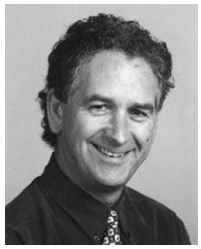

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Dr. Hayes-Gill is a member of the IEE.